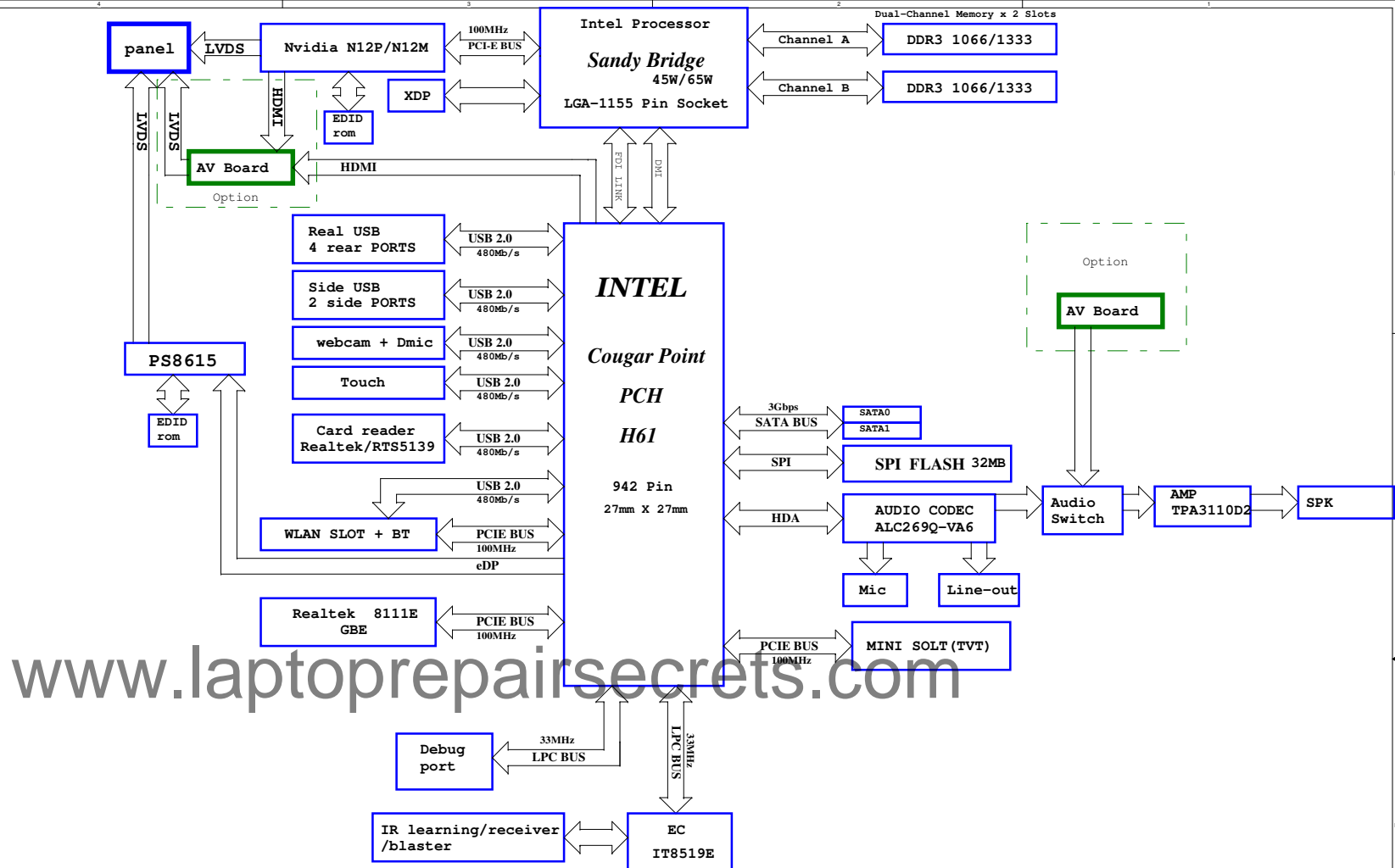
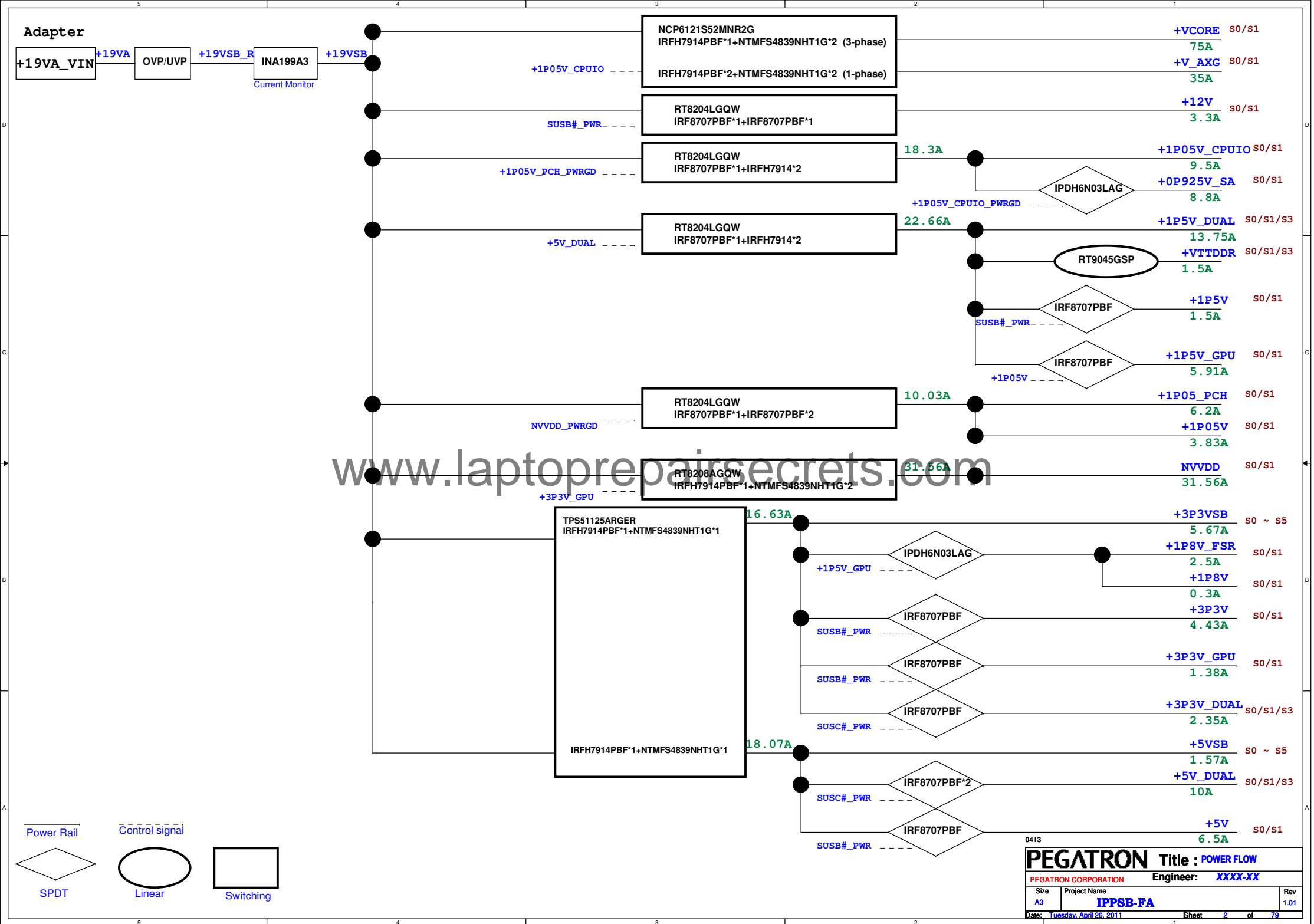
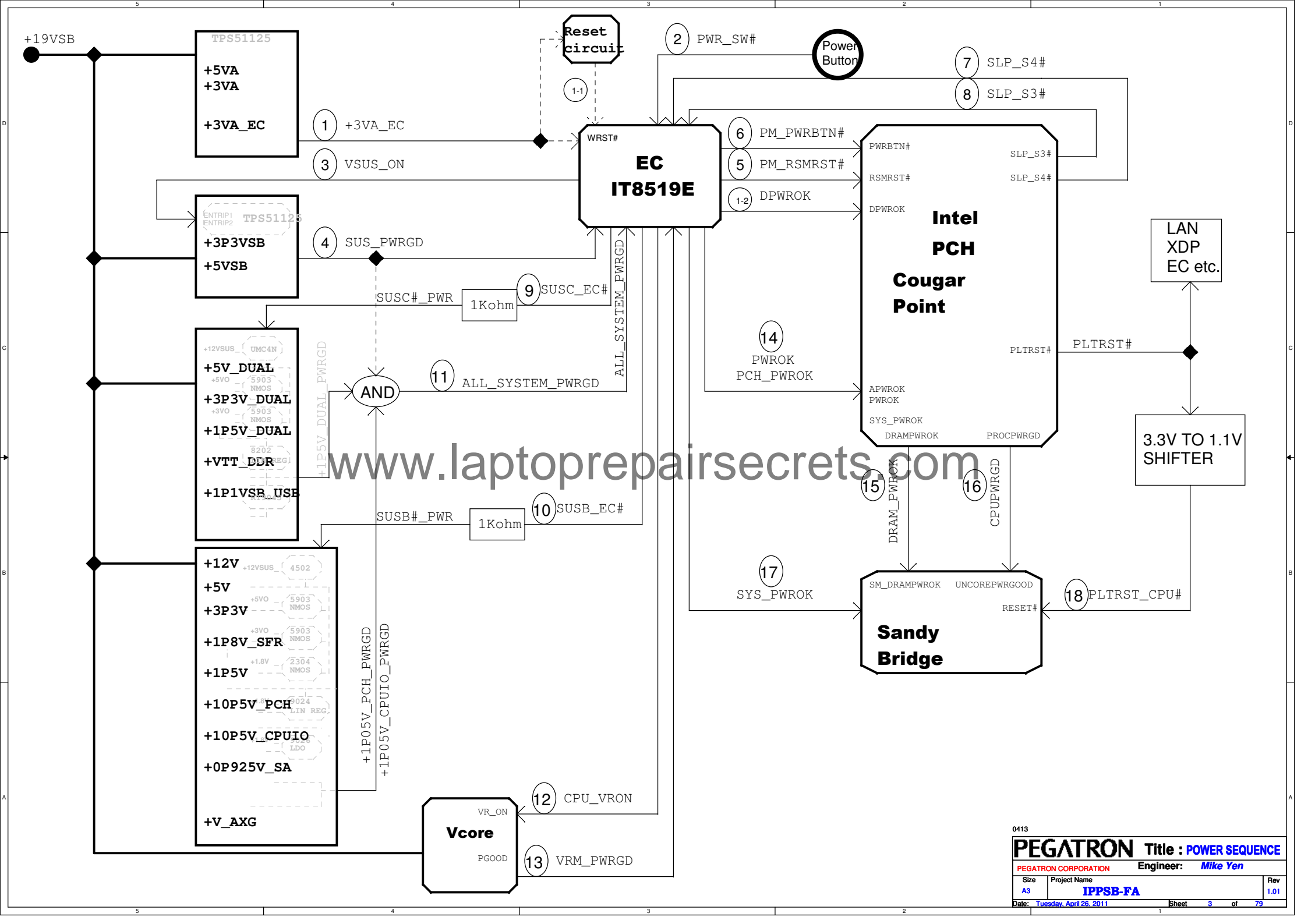


IPPSB-FA

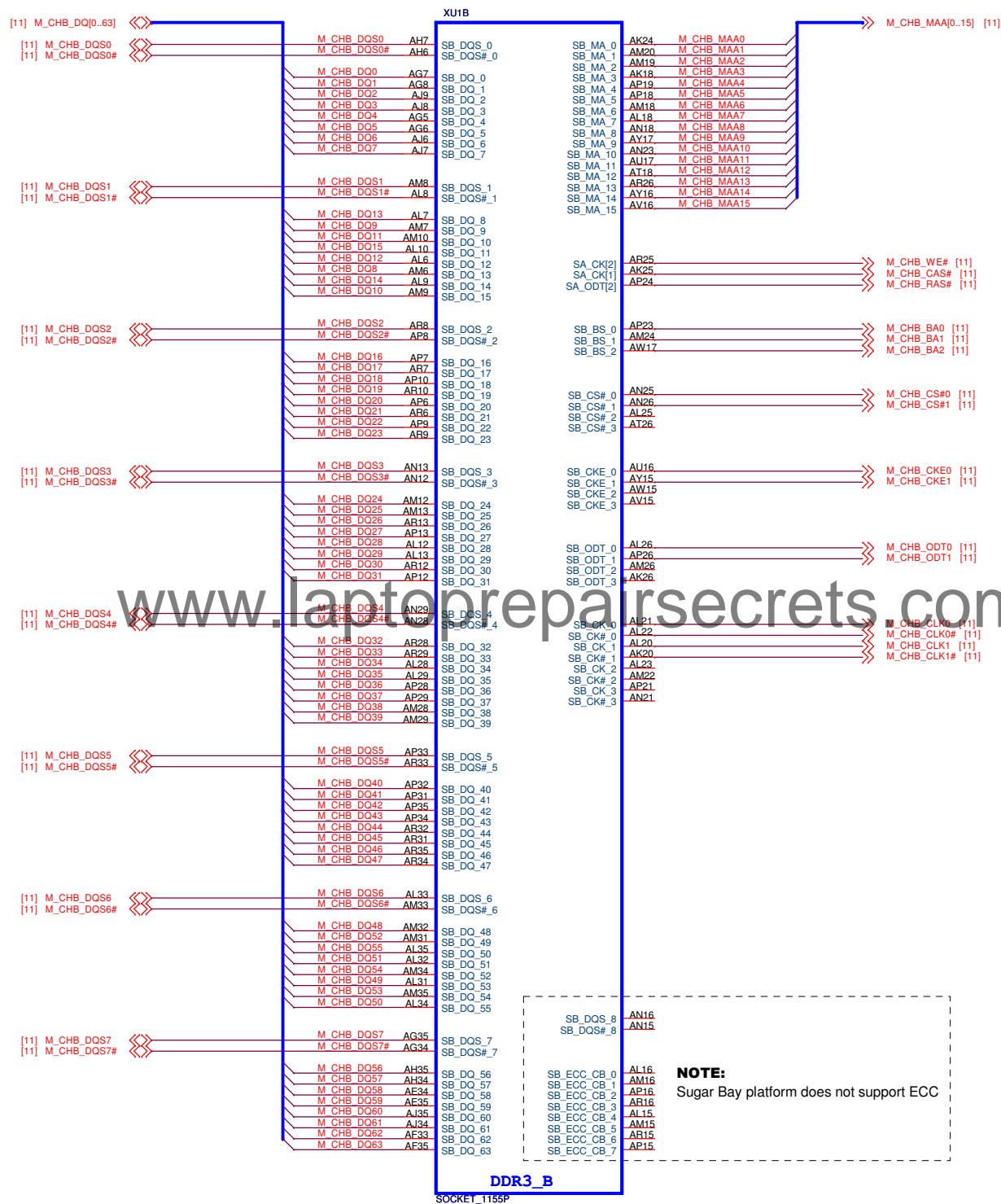
| PAGE | TITLE |
|-------|-----------------------------|
| 01 | BLOCK DIAGRAM |
| 02 | POWER FLOW |
| 03 | POWER SEQUENCE |
| 04~09 | CPU LGA1155 DDR3 A 1-6 |
| 10 | DDR3 CHANNEL A G/F |
| 11 | DDR3 CHANNEL B G/F |
| 12 | DDR3 TERMINATION A&B |
| 13 | PLTRST CPU# & Smbus |
| 14 | Converter Controller |
| 15~16 | LVDS&AV CONN |
| 17~25 | INTEL_PCH 1-9 |
| 27~28 | LAN |
| 29~30 | CODEC&CONN |
| 31~32 | AMP&SWITCH |
| 33~35 | USB&HUB&BT |
| 36 | HPD_DET |
| 37~38 | MINI_CARD (WL&TVT&DMC) |
| 39 | Misc. conn&Touch&Wcam&RTC |
| 40 | FAN |
| 41 | PWR_LED & Button* |
| 42 | IR_LEDS |
| 43~44 | EC 8519 |
| 45 | SM_BUS & SPI_ROM |
| 46 | SCREW_HOLE |
| 47 | UVF, OVP, & +19VSB |
| 48 | LOAD_SWITCH |
| 49 | +3P3VSB&+5VSB |
| 50 | +1P5V_DUAL & +1P2V |
| 51 | Current Monitor |
| 52 | +12V & +1P8V |
| 53 | +1P05V_CPUIO&+0P925V_SA |
| 54 | POWER_PROTECT |
| 55 | +1P05V_CPUIO_CAP |
| 56 | +VTT_DDR |
| 57 | +V_AXG_DRIVER |
| 58 | +VCORE_CONTROLLER |
| 59~61 | +VCORE_CAP |
| 62 | +1P05V&+1P05V_PCH |
| 63~64 | CPU&PCH_XDP_DEBUG_CONNECTOR |
| 65 | VGA_CONN |
| 66~67 | GPU_DDR3 |
| 68 | VGA-N12P_STRAPPING+EEPROM |
| 69 | MXM.VGA-N12P_Xtal/Thermal |
| 70~71 | GPU_HDMI (DMC&AV) |
| 72 | GPU_CTRL |
| 73 | GPU.VGA_N12P_PCI-E I/F |
| 74 | GPU_PCI-E_LVDS_VGA |
| 75 | MXM.GPU_Discharge |
| 76 | GPU_POWER&GND |
| 77 | MXM.NVDD |
| 78 | Card Reader RTS5139-GR |
| 79 | EDP_CH7511 |

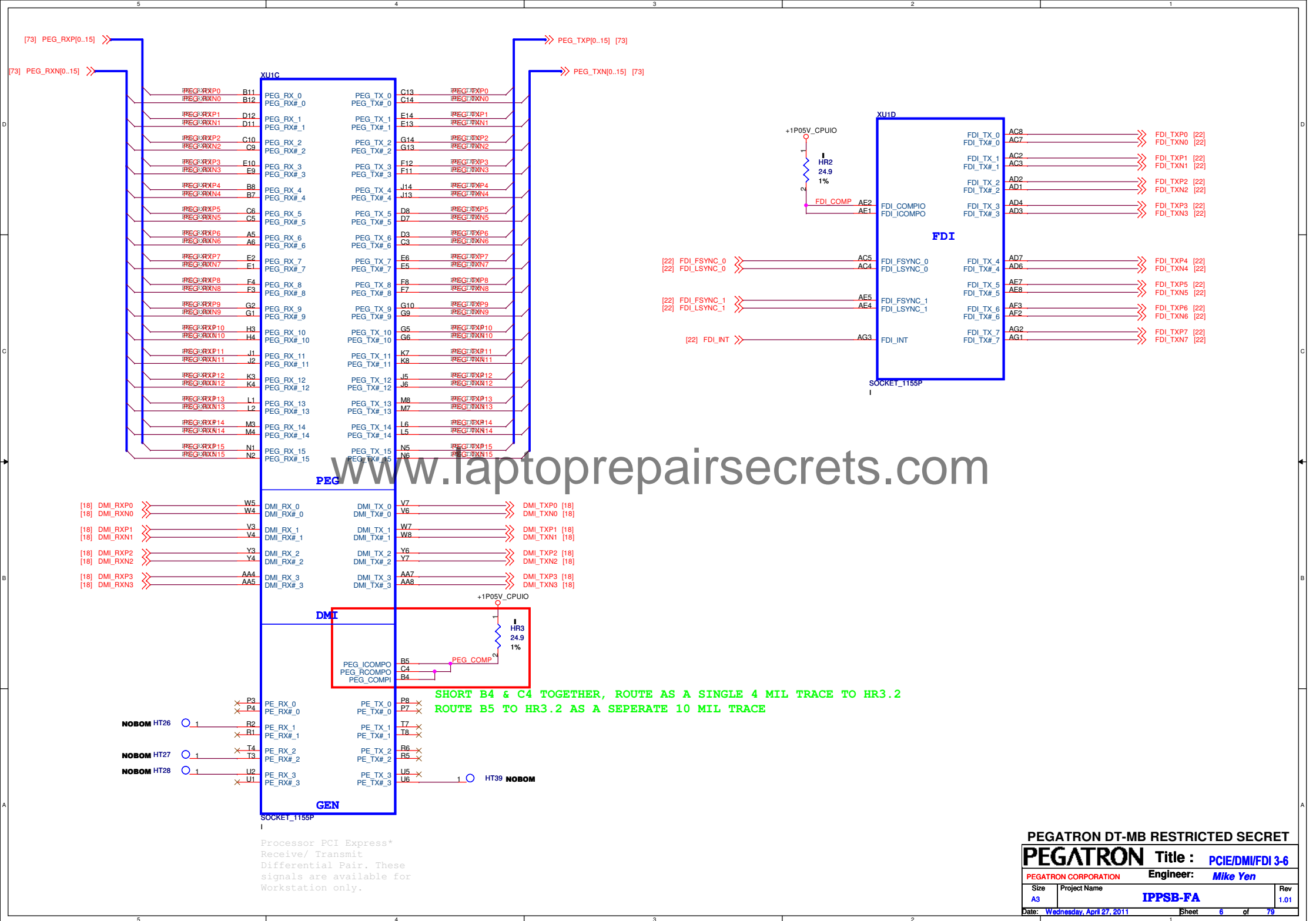


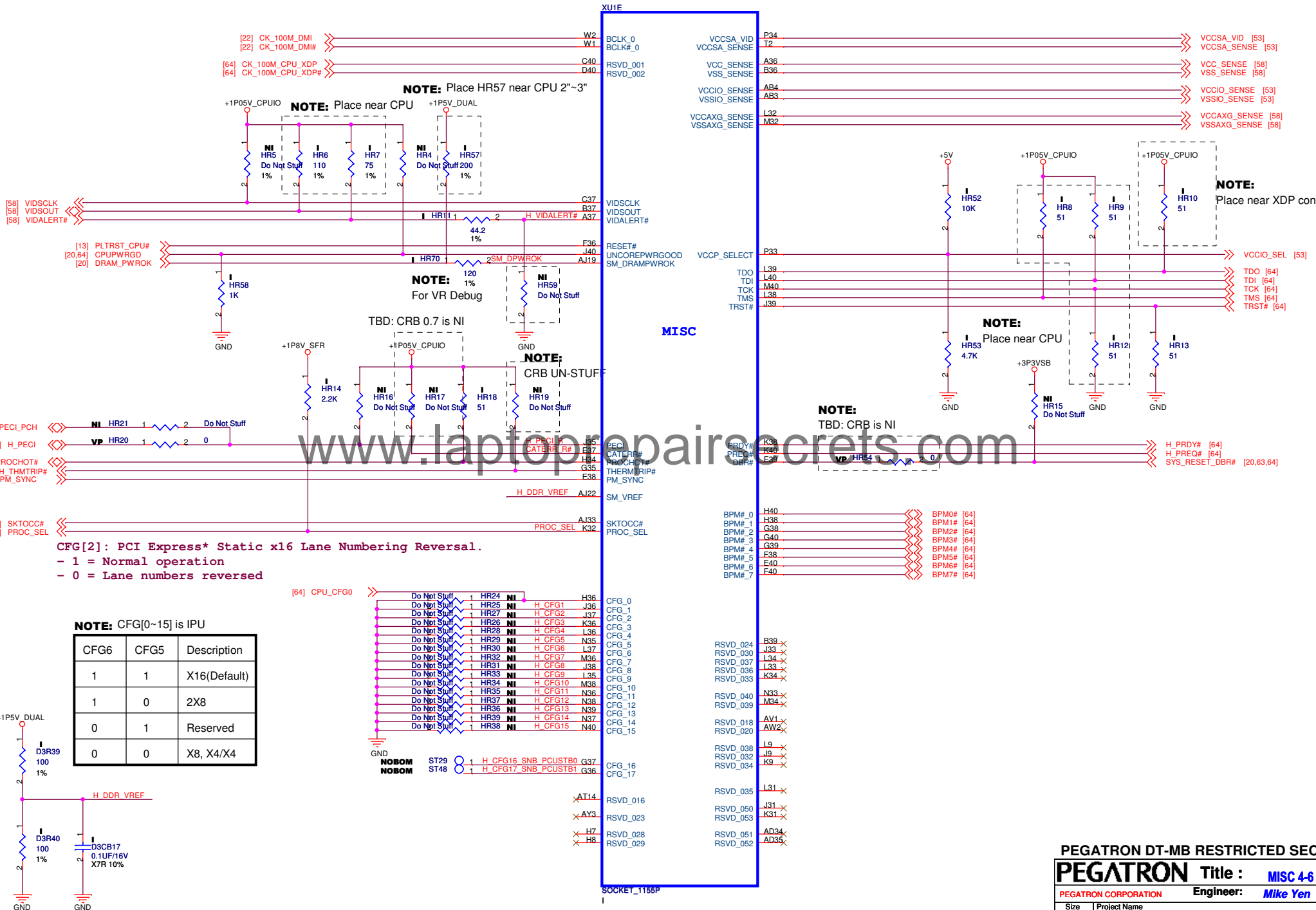




Date: Wednesday, April 27, 2011 Sheet 4 of 79







NOTE: Place HR57 near CPU 2"-3"

NOTE: Place near CPU

NOTE: Place near XDP connector

NOTE: For VR Debug

NOTE: CRB UN-STUFF

NOTE: TBD: CRB is NI

NOTE: Place near CPU

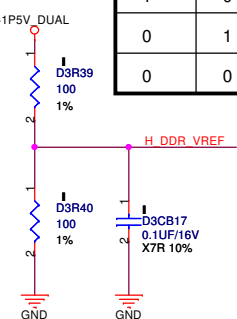
CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
- 1 = Normal operation
- 0 = Lane numbers reversed

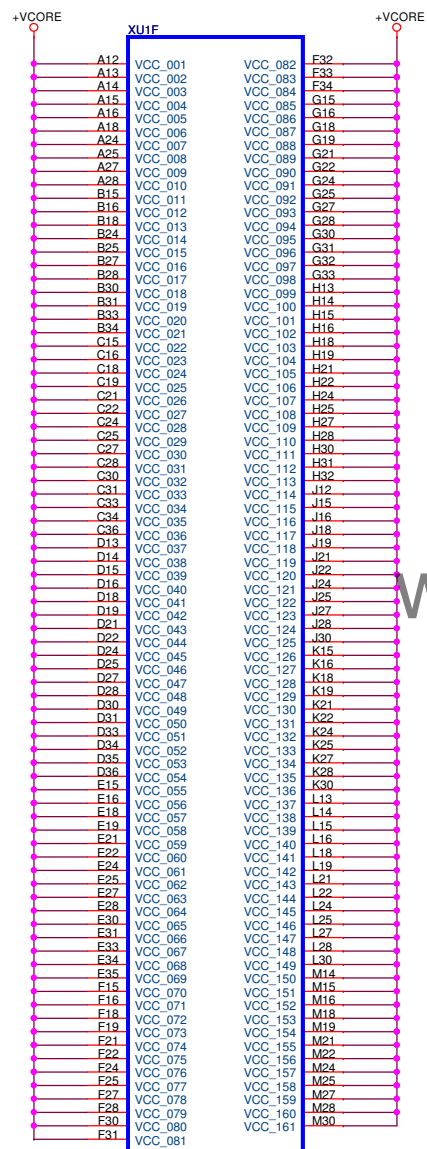
NOTE: CFG[0~15] is IPU

| CFG6 | CFG5 | Description |
|------|------|--------------|
| 1 | 1 | X16(Default) |
| 1 | 0 | 2X8 |
| 0 | 1 | Reserved |
| 0 | 0 | X8, X4/X4 |

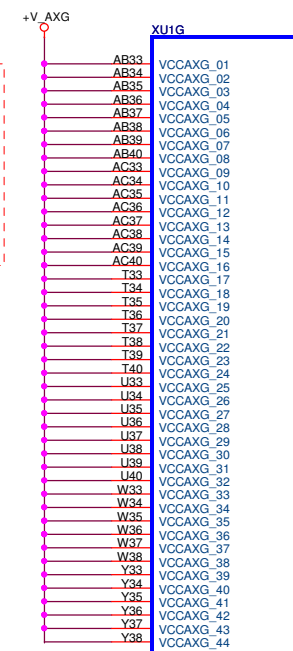
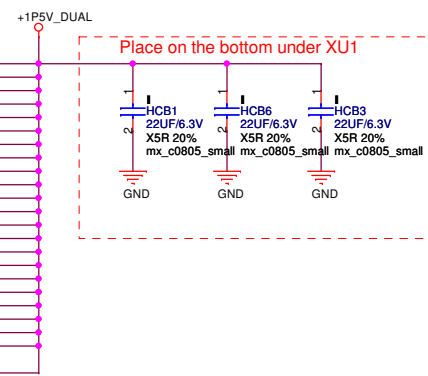
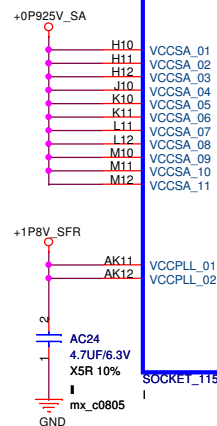
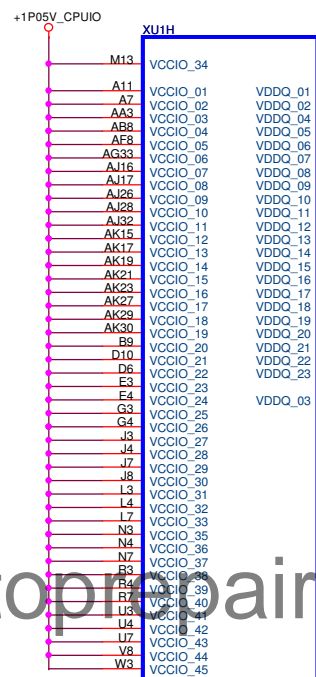
| | | | | | | |
|---------------|--------------|---|------|----|-----|--------|
| [64] CPU_CFG0 | Do Not Stuff | 1 | HR24 | NI | H36 | CFG_0 |
| | Do Not Stuff | 1 | HR25 | NI | H36 | CFG_1 |
| | Do Not Stuff | 1 | HR27 | NI | H37 | CFG_2 |
| | Do Not Stuff | 1 | HR26 | NI | H36 | CFG_3 |
| | Do Not Stuff | 1 | HR28 | NI | H36 | CFG_4 |
| | Do Not Stuff | 1 | HR29 | NI | H35 | CFG_5 |
| | Do Not Stuff | 1 | HR30 | NI | H37 | CFG_6 |
| | Do Not Stuff | 1 | HR32 | NI | H36 | CFG_7 |
| | Do Not Stuff | 1 | HR31 | NI | H38 | CFG_8 |
| | Do Not Stuff | 1 | HR33 | NI | H35 | CFG_9 |
| | Do Not Stuff | 1 | HR34 | NI | H38 | CFG_10 |
| | Do Not Stuff | 1 | HR35 | NI | H36 | CFG_11 |
| | Do Not Stuff | 1 | HR37 | NI | H38 | CFG_12 |
| | Do Not Stuff | 1 | HR36 | NI | H39 | CFG_13 |
| | Do Not Stuff | 1 | HR39 | NI | H37 | CFG_14 |
| | Do Not Stuff | 1 | HR38 | NI | H40 | CFG_15 |

NOBOM ST29 1 H_CFG16_SNB_PCUSTB0 G37
NOBOM ST48 1 H_CFG17_SNB_PCUSTB1 G36





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SOCKET_T1155P

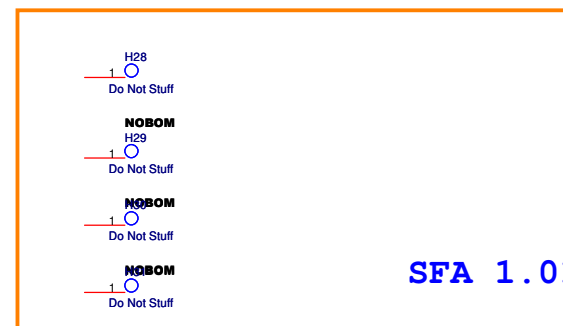
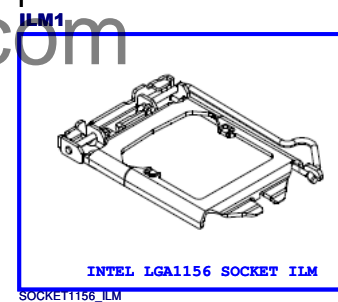
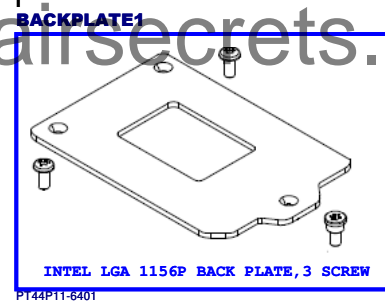
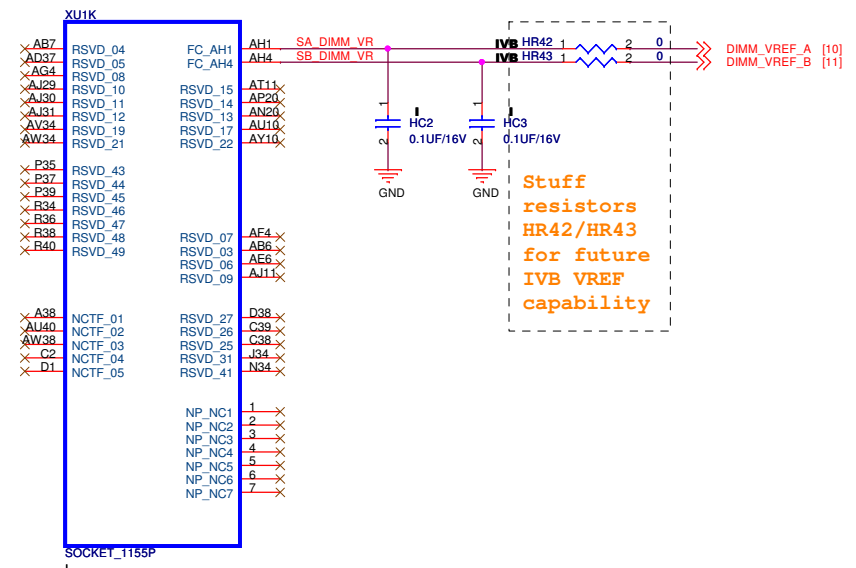
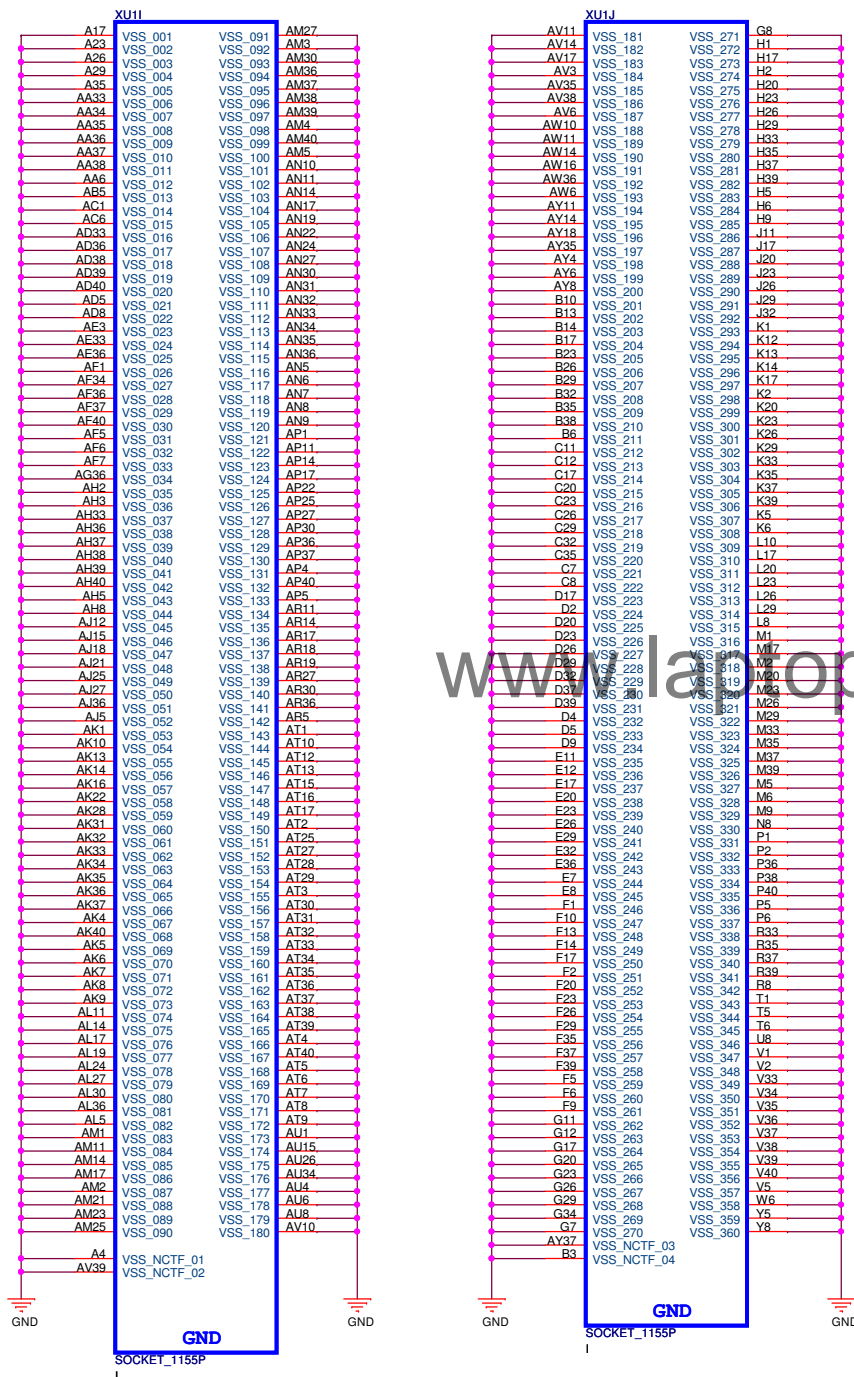
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **VCC 5-6**

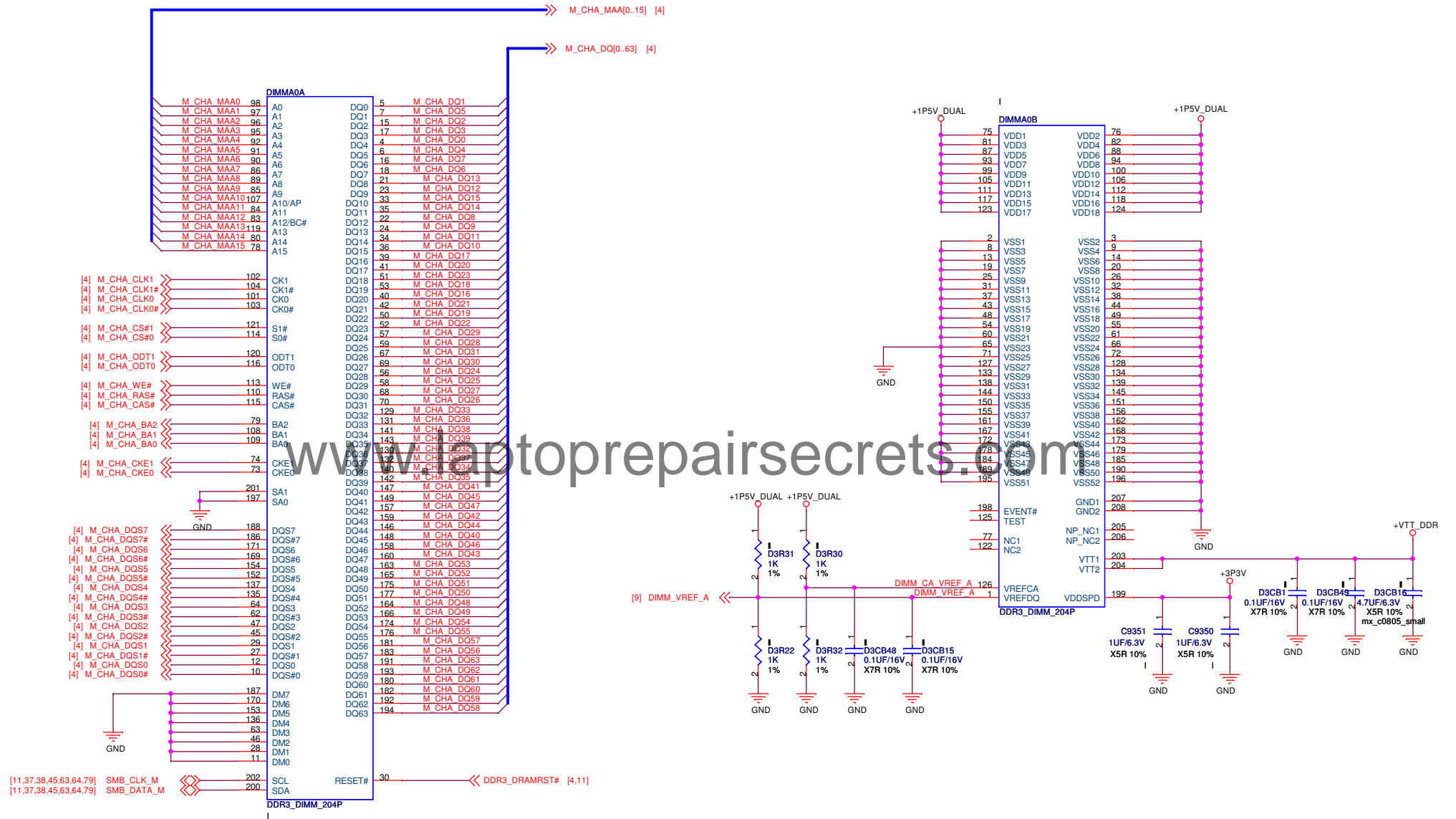
PEGATRON CORPORATION Engineer: **Mike Yen**

Size **A3** Project Name **IPPSB-FA** Rev **1.01**

Date: **Tuesday, April 26, 2011** Sheet **8** of **79**



皆改爲5.2H

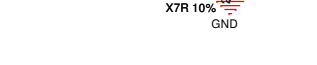
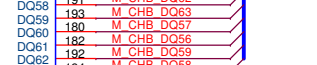
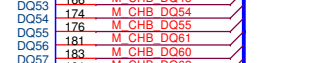
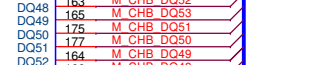
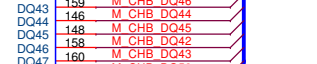
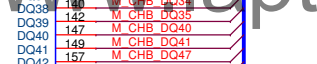
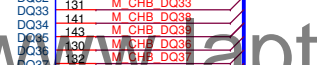
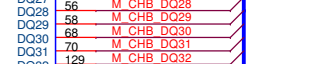
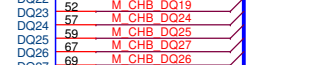
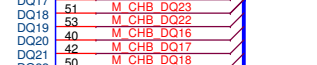
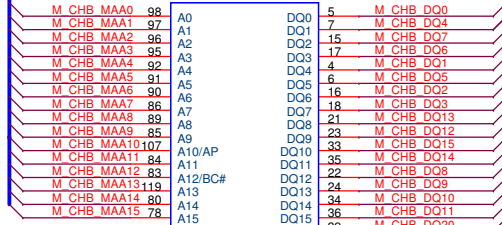


皆改為5.2H

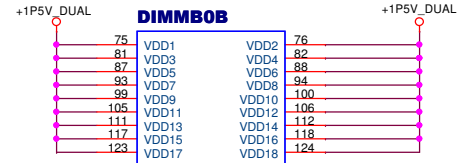
M_CHB_DQ[0..63] [5]

M_CHB_MAA[0..15] [5]

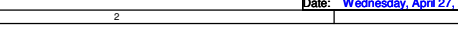
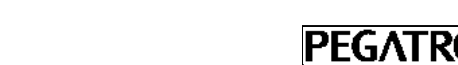
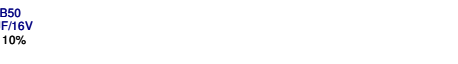
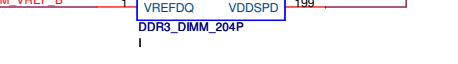
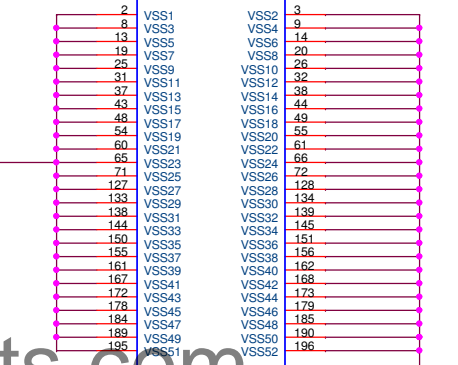
(5.2H)
DIMMB0A



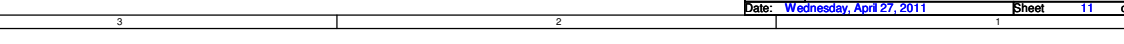
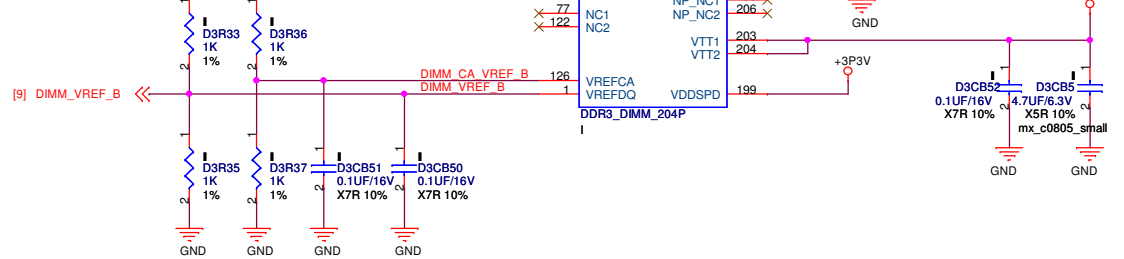
DIMMB0B

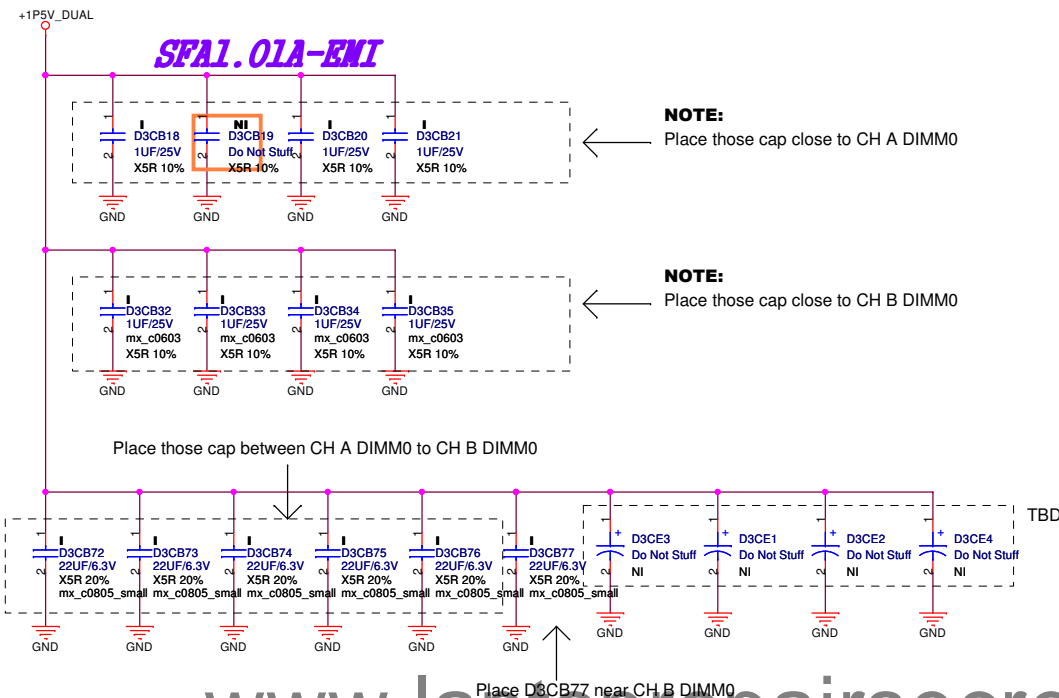


GND



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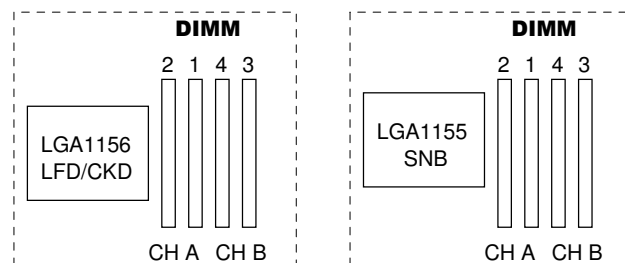




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NOTE:

DIMM Placement for different platform



PEGATRON DT-MB RESTRICTED SECRET

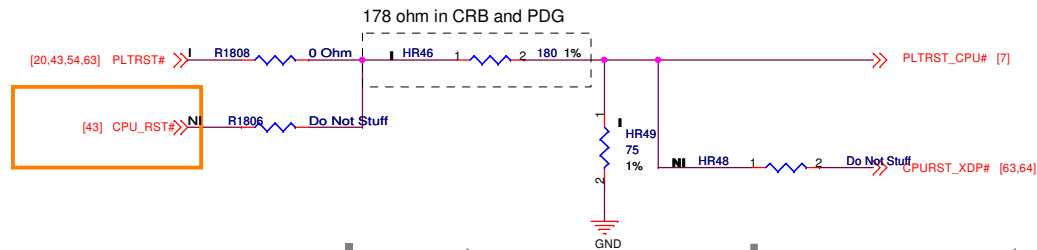
PEGATRON Title : DDR3 TERMINATION A&B

PEGATRON CORPORATION Engineer: Mike Yen

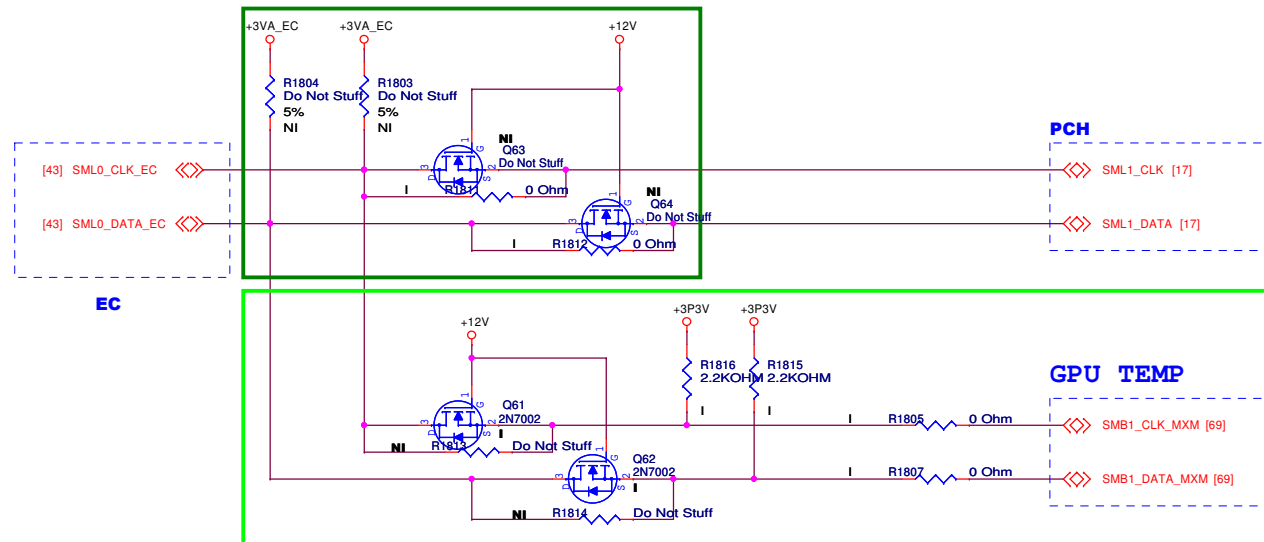
| | | |
|------------|--------------------------|-------------|
| Size A3 | Project Name IPPSB-FA | Rev 1.01 |
|------------|--------------------------|-------------|

Date: Tuesday, April 26, 2011 Sheet 12 of 79

PLTRST_CPU#



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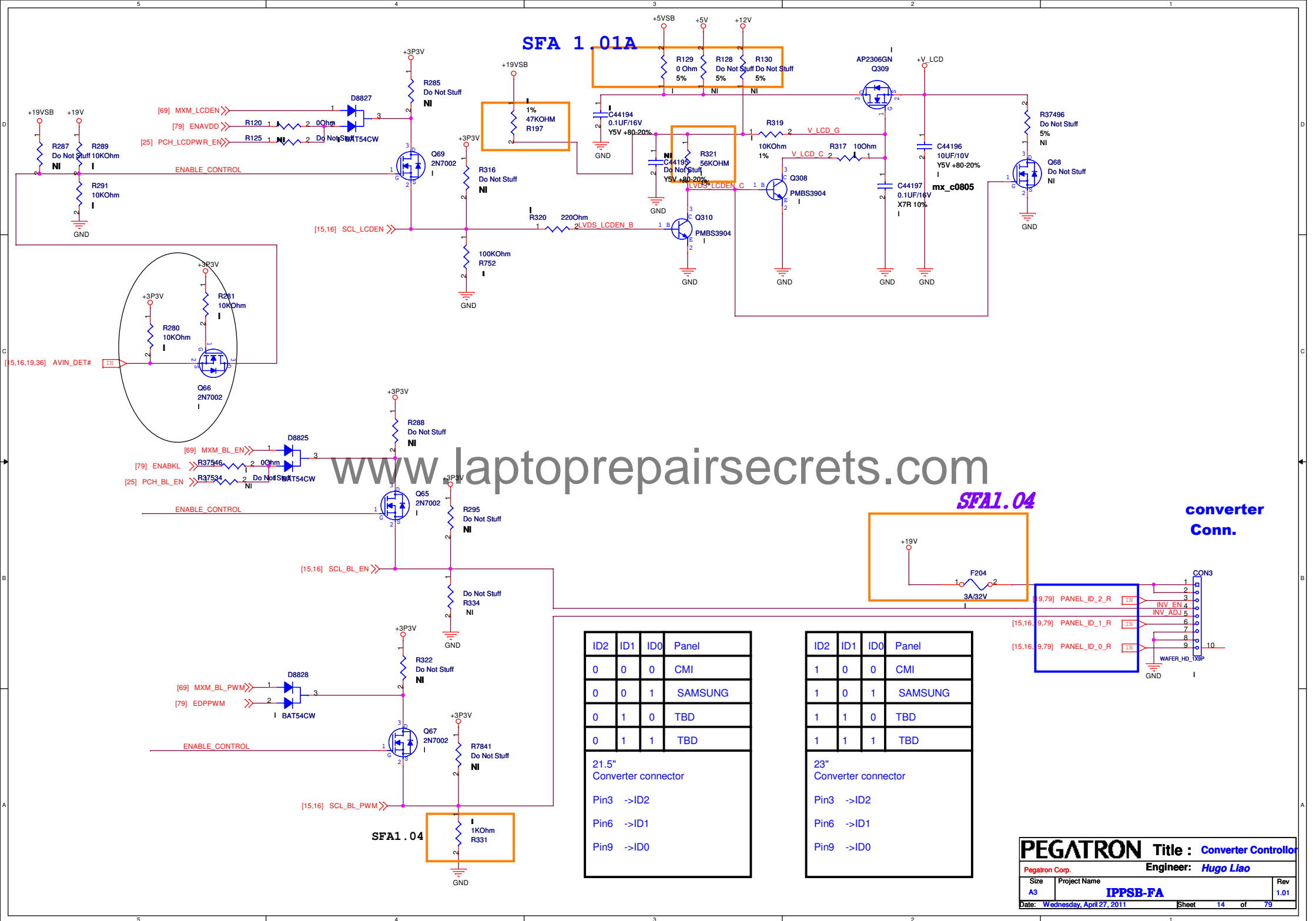
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PLTRST_CPU#&SMBus

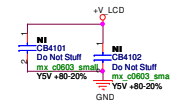
PEGATRON CORPORATION Engineer: XXXX-XX

| | | |
|------------|---------------------------------|-------------|
| Size A3 | Project Name IPPSB-FA | Rev 1.01 |
|------------|---------------------------------|-------------|

Date: Wednesday, April 27, 2011 Sheet 13 of 79



LCD CONN NB & GPU colay

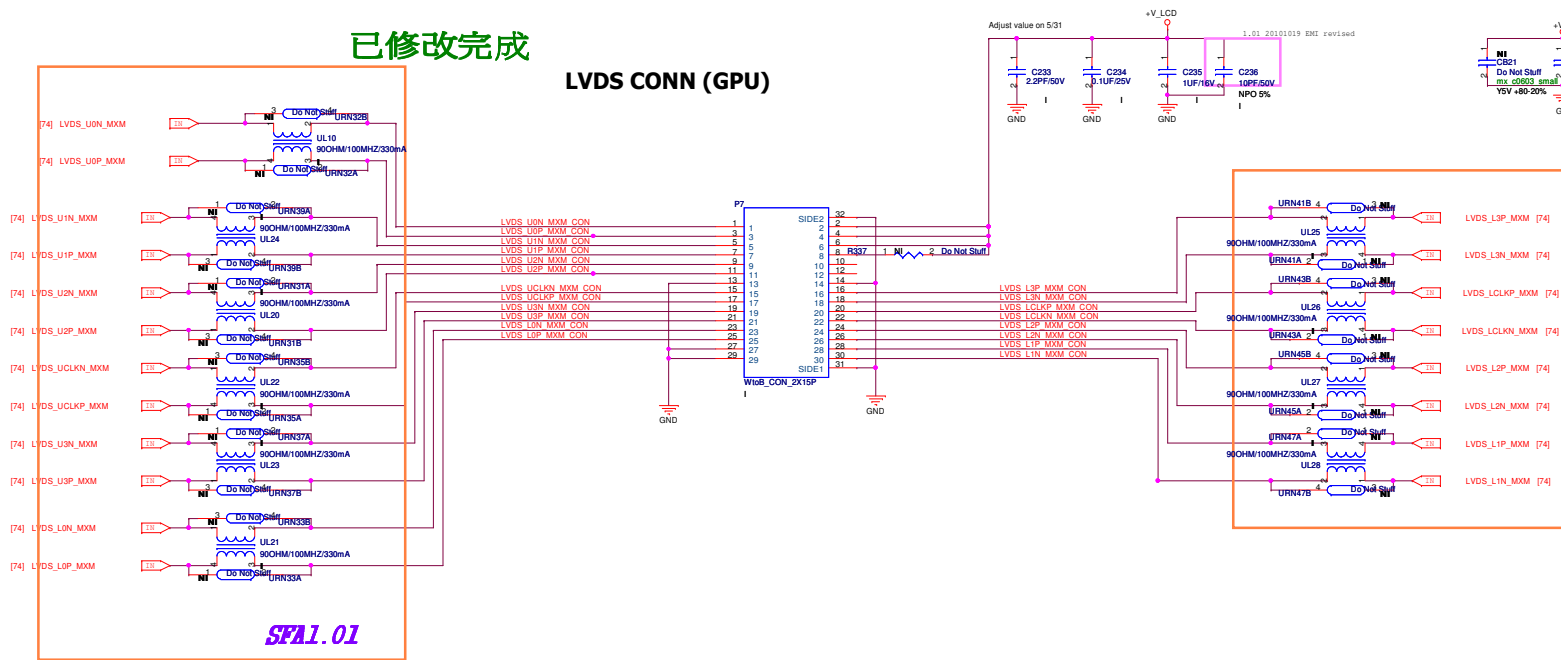


AV Board connector (PCH)

[illegible]

已修改完成

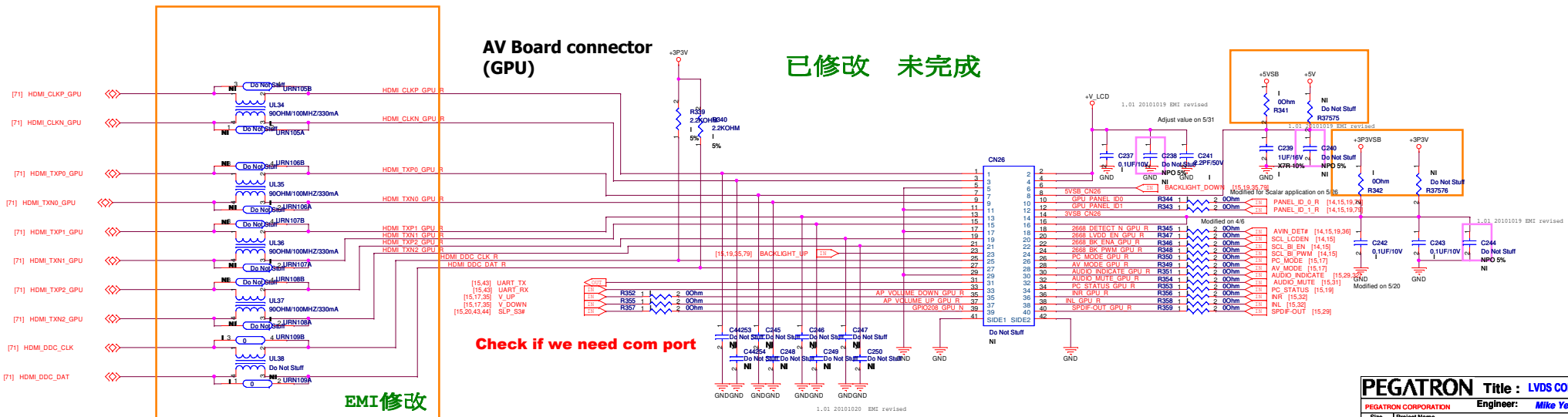
LVDS CONN (GPU)



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AV Board connector (GPU)

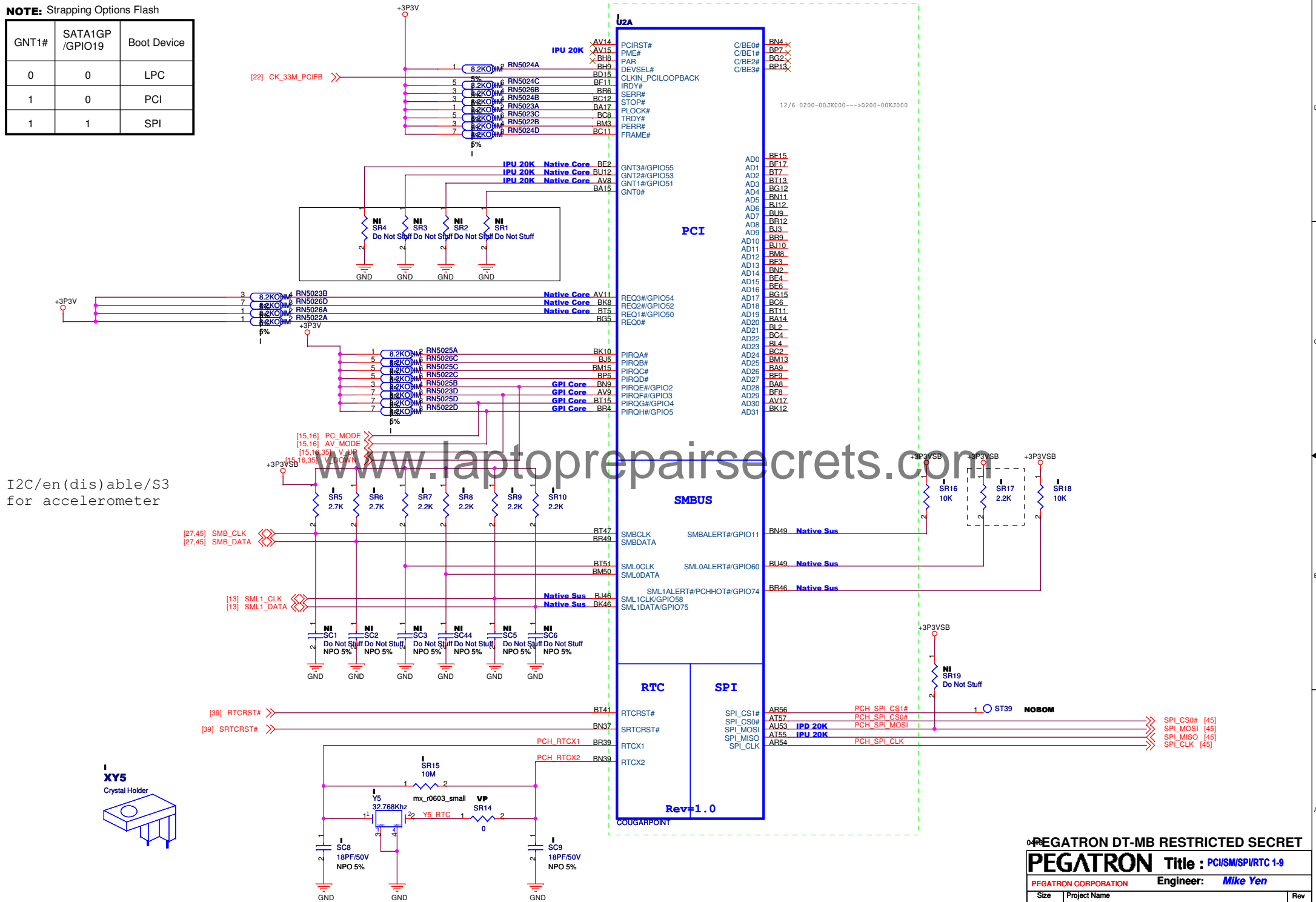
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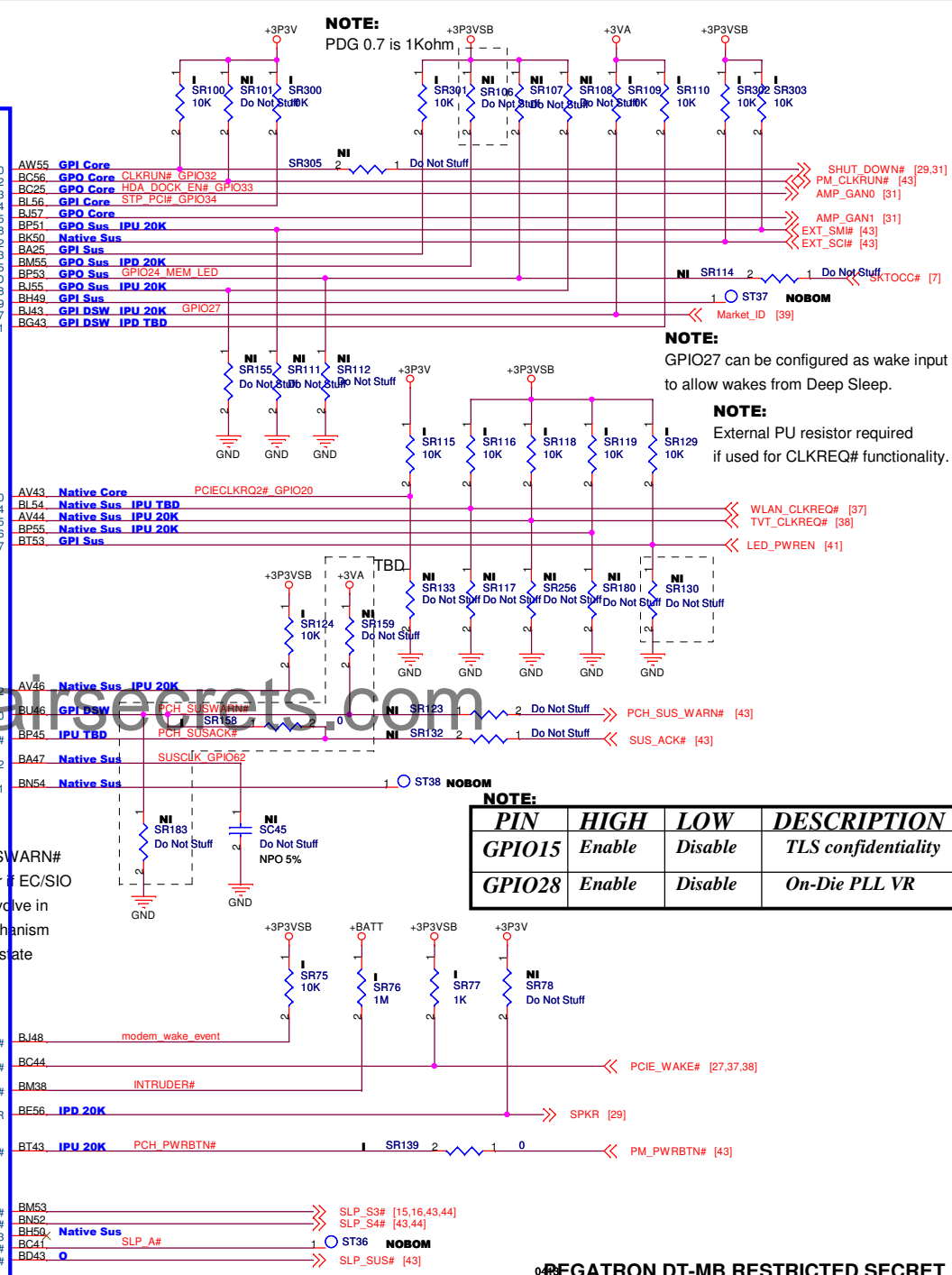
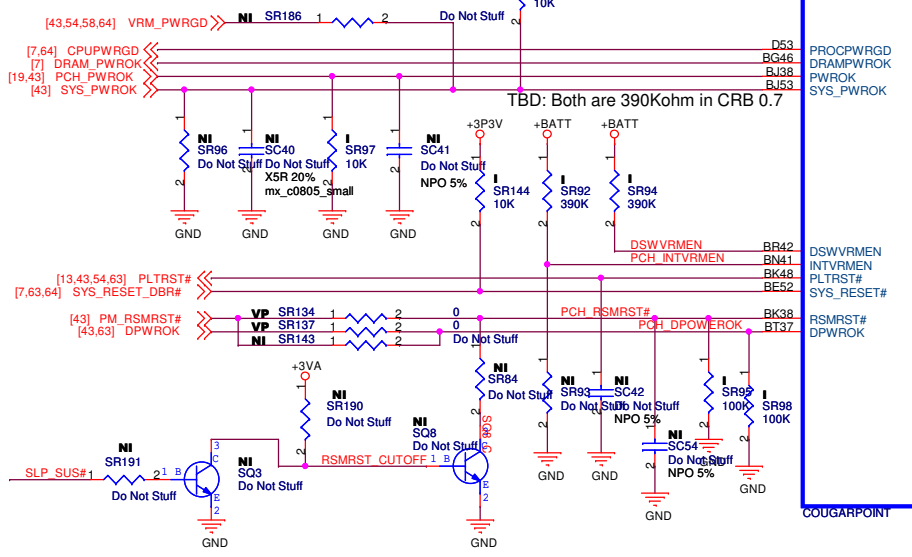


Check if we need com port

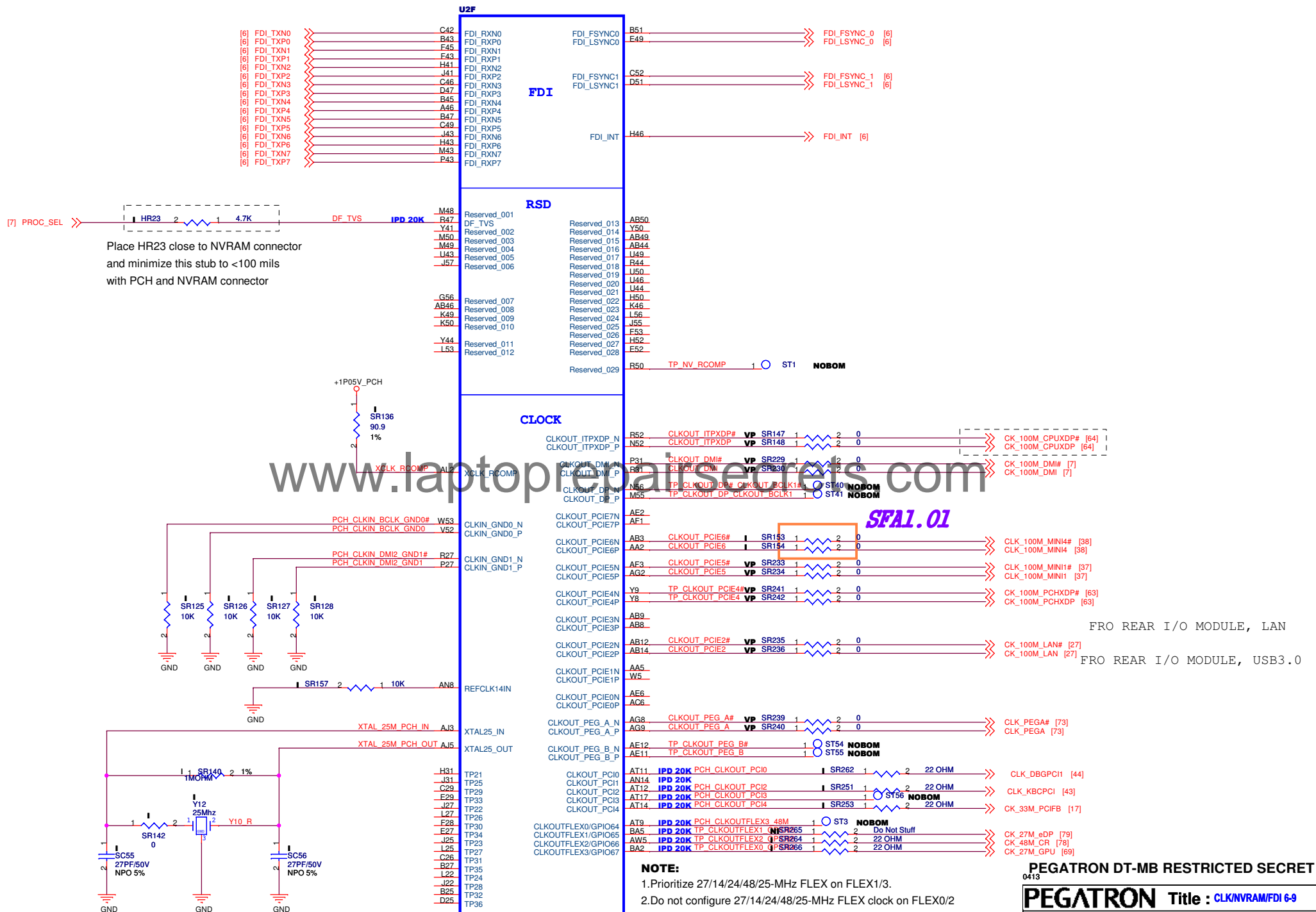
| PEGATRON | | Title : LVDS CON | |
|----------------------|---------------------------------|--------------------|----------|
| PEGATRON CORPORATION | | Engineer: Mike Yan | |
| Size | Project Name | IPSPB-FA | Rev 1.01 |
| A2 | Date: Wednesday, April 27, 2011 | Sheet 16 of 29 | |

| GNT1# | SATA1GP /GPIO19 | Boot Device |
|-------|--------------------|-------------|
| 0 | 0 | LPC |
| 1 | 0 | PCI |
| 1 | 1 | SPI |





| PIN | HIGH | LOW | DESCRIPTION |
|---------------|---------------|----------------|----------------------------|
| GPIO15 | <i>Enable</i> | <i>Disable</i> | <i>TLS confidentiality</i> |
| GPIO28 | <i>Enable</i> | <i>Disable</i> | <i>On-Die PLL VR</i> |



NOTE:

1. Prioritize 27/14/24/48/25-MHz FLEX on FLEX1/3.
2. Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0/2 if more than 2 PCI clocks + PCI loopback are routed.
3. With 2 PCI clocks routed (or less), prioritize the FLEX clocks to FLEX1/3
a. 27MHz(SSC/non-SSC) b. 14.31818MHz c. 24/48 d. 25MHz

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CLKNVRAM/FDI 6-9

PEGATRON CORPORATION Engineer: Mike Yen

Size A3 Project Name IPPSB-FA Rev 1.01

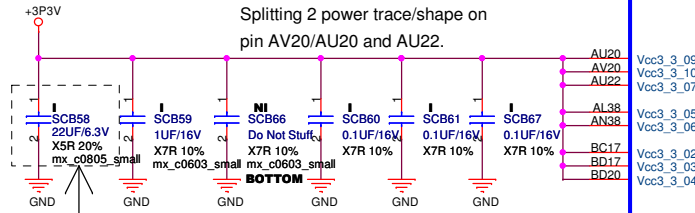
Date: Wednesday, April 27, 2011 Sheet 22 of 79

NOTE:

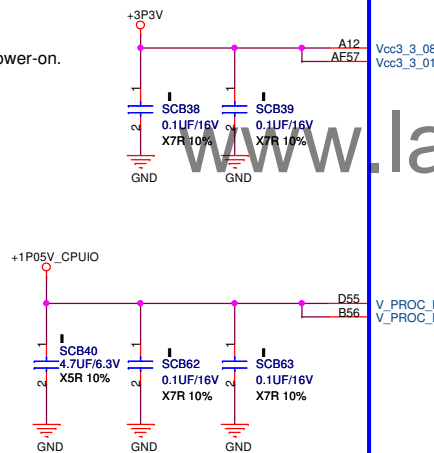
Place SCB59 and SCB66 near pin AU20,
SCB60 near pin AL38,
SCB61 and SCB67 near BC17.

NOTE:

Splitting 2 power trace/shape on
pin AV20/AU20 and AU22.

**NOTE:**

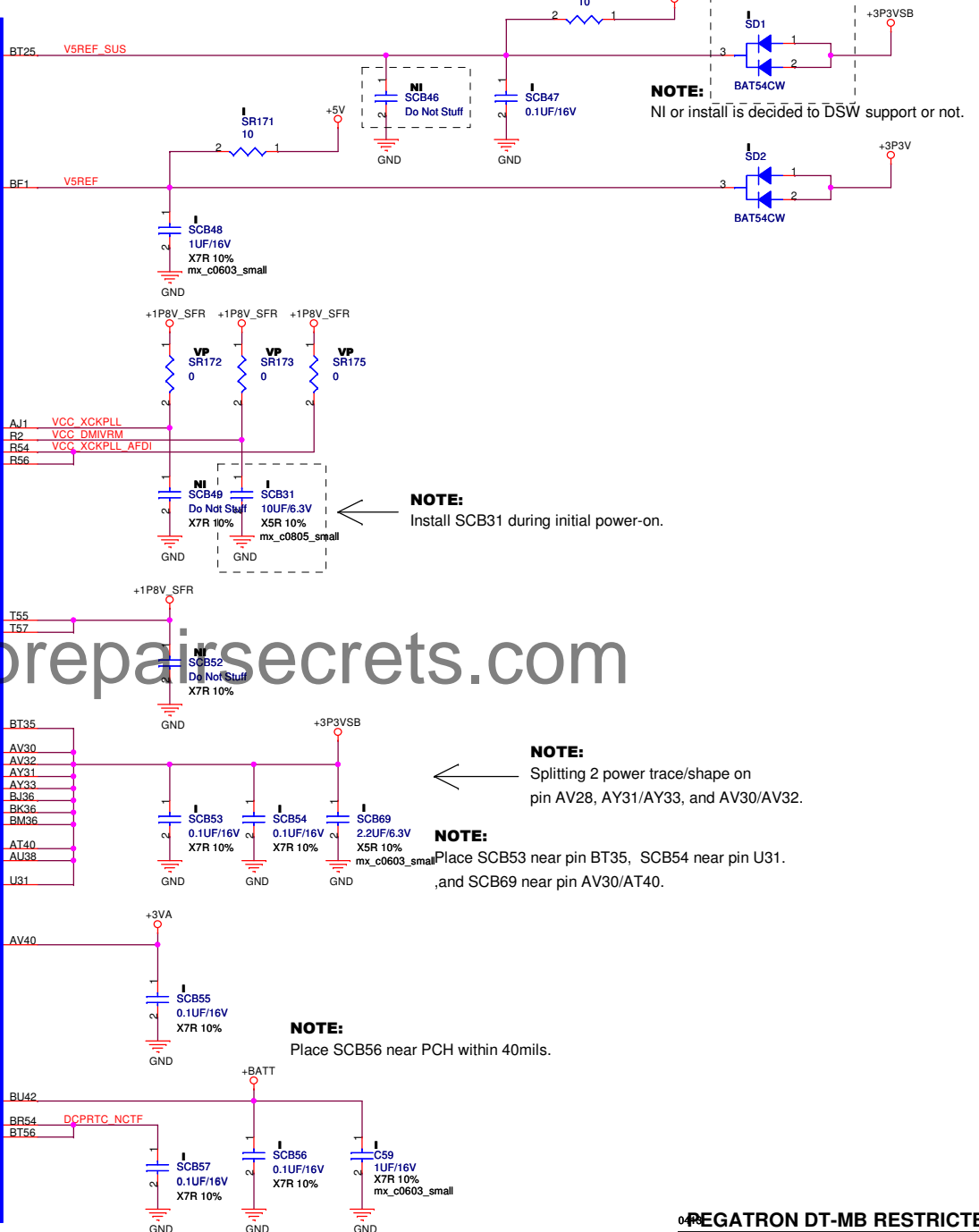
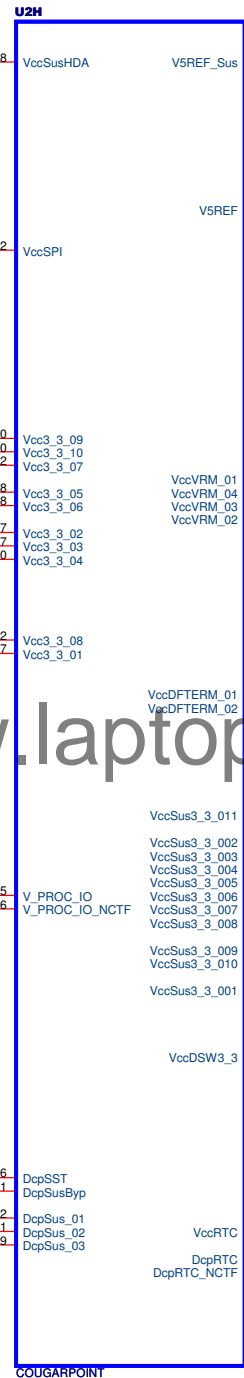
Install SCB58 during initial power-on.

**NOTE:**

Just for measurement.

CRB 0.7 is 1uF

COUGARPOINT

**NOTE:**

NI or install is decided to DSW support or not.

NOTE:

Install SCB31 during initial power-on.

NOTE:

Splitting 2 power trace/shape on
pin AV28, AY31/AY33, and AV30/AV32.

NOTE:

Place SCB53 near pin BT35, SCB54 near pin U31,
and SCB69 near pin AV30/AT40.

NOTE:

Place SCB56 near PCH within 40mils.

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VCCSUS 8-9

PEGATRON CORPORATION Engineer: Mike Yen

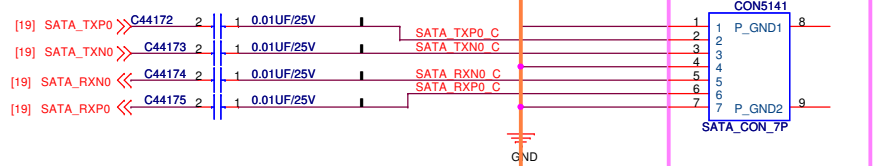
Size A3 Project Name IPPSB-FA

Date: Tuesday, April 26, 2011 Sheet 24 of 79

已更改完成

SATA HDD CON

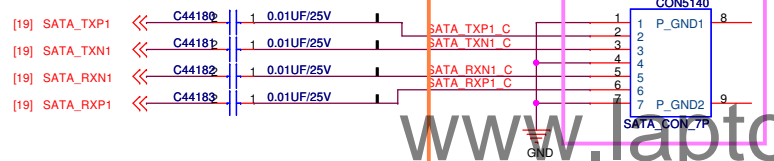
1.01 20101019 revised



**SATA CONTROLLER #1
(MASTER)
COLOR = DARK BLUE**

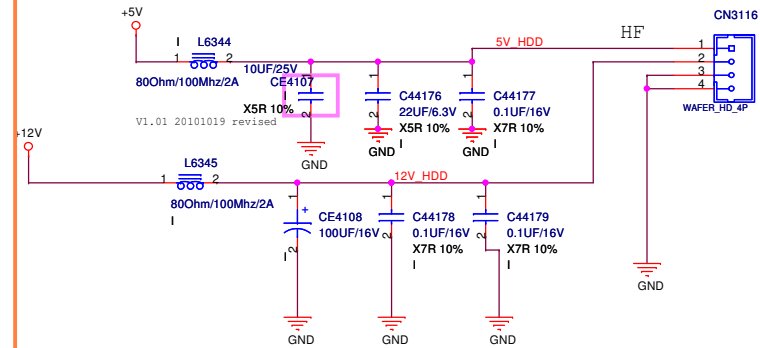
SATA ODD CON

1.01 20101019 revised

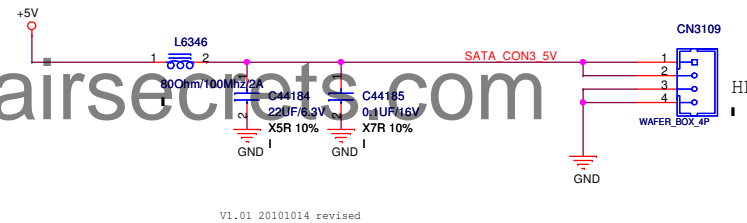


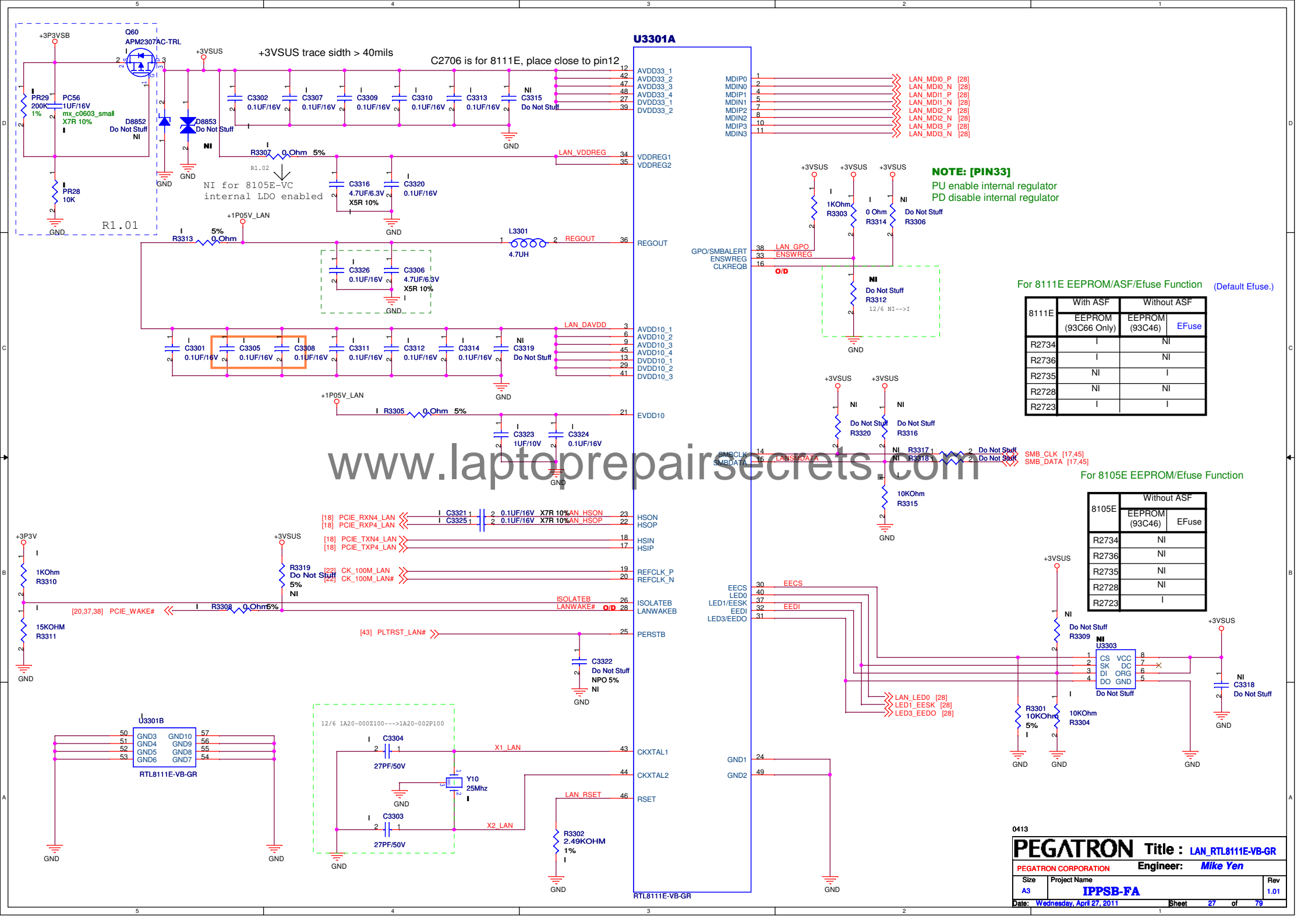
**SATA CONTROLLER #2
(SLAVE)
COLOR = WHITE**

SATA POWER CONN.



ODD POWER CONN.





For 8111E EEPROM/ASF/Efuse Function (Default Efuse.)

| 8111E | With ASF | Without ASF |
|-------|---------------------|----------------------|
| | EEPROM (93C66 Only) | EEPROM (93C46) EFuse |
| R2734 | I | NI |
| R2736 | I | NI |
| R2735 | NI | I |
| R2728 | NI | NI |
| R2723 | I | I |

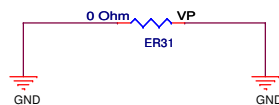
For 8105E EEPROM/Efuse Function

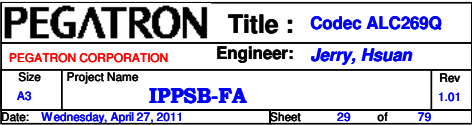
| 8105E | Without ASF |
|-------|----------------------|
| | EEPROM (93C46) EFuse |
| R2734 | NI |
| R2736 | NI |
| R2735 | NI |
| R2728 | NI |
| R2723 | I |

SFA1.01A

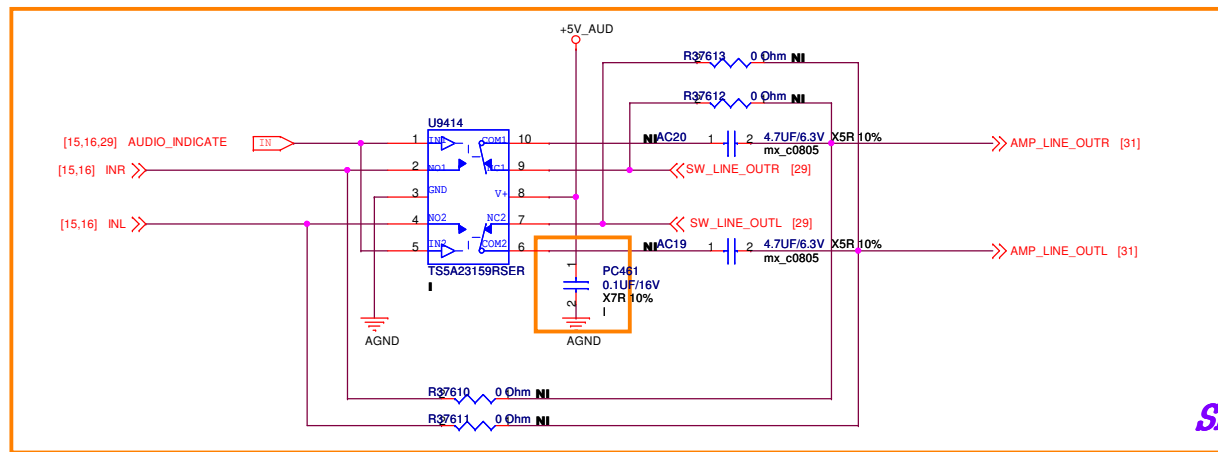


| | | |
|----------|-------------------|----------------------|
| State | LINK Green LED | Yellow LED ACTIVE |
| S0 | ON | OFF or blinking |
| S1,S3,S4 | OFF | OFF |



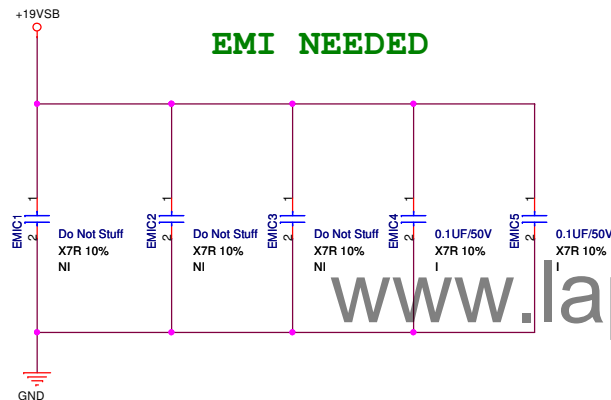




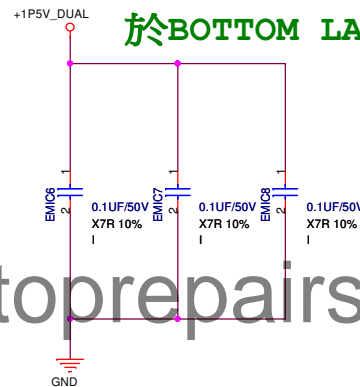


SFA1.04

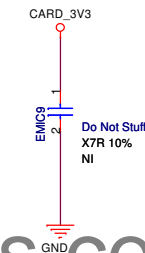
EMI NEEDED



於BOTTOM LAYER 上

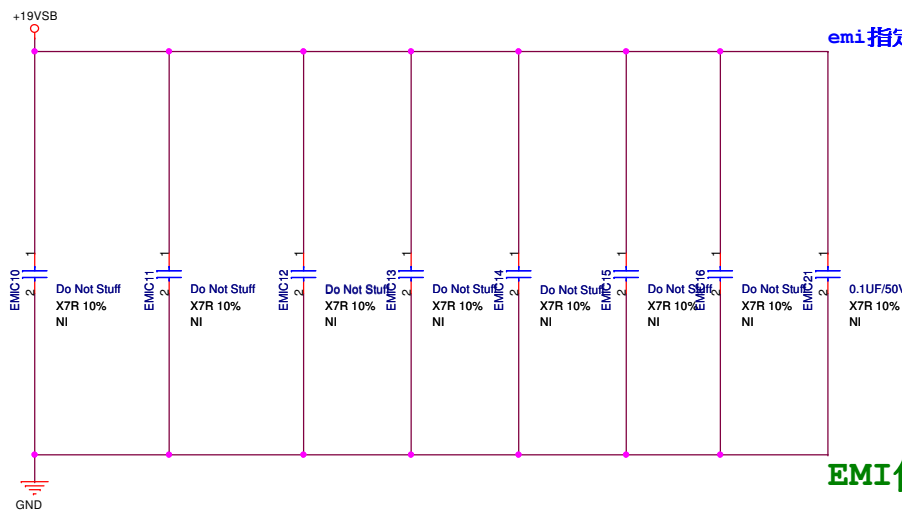


於TOP LAYER 上



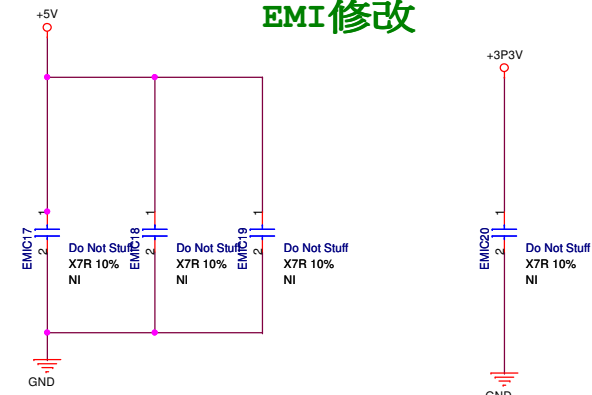
www.laptoprepairsecrets.com

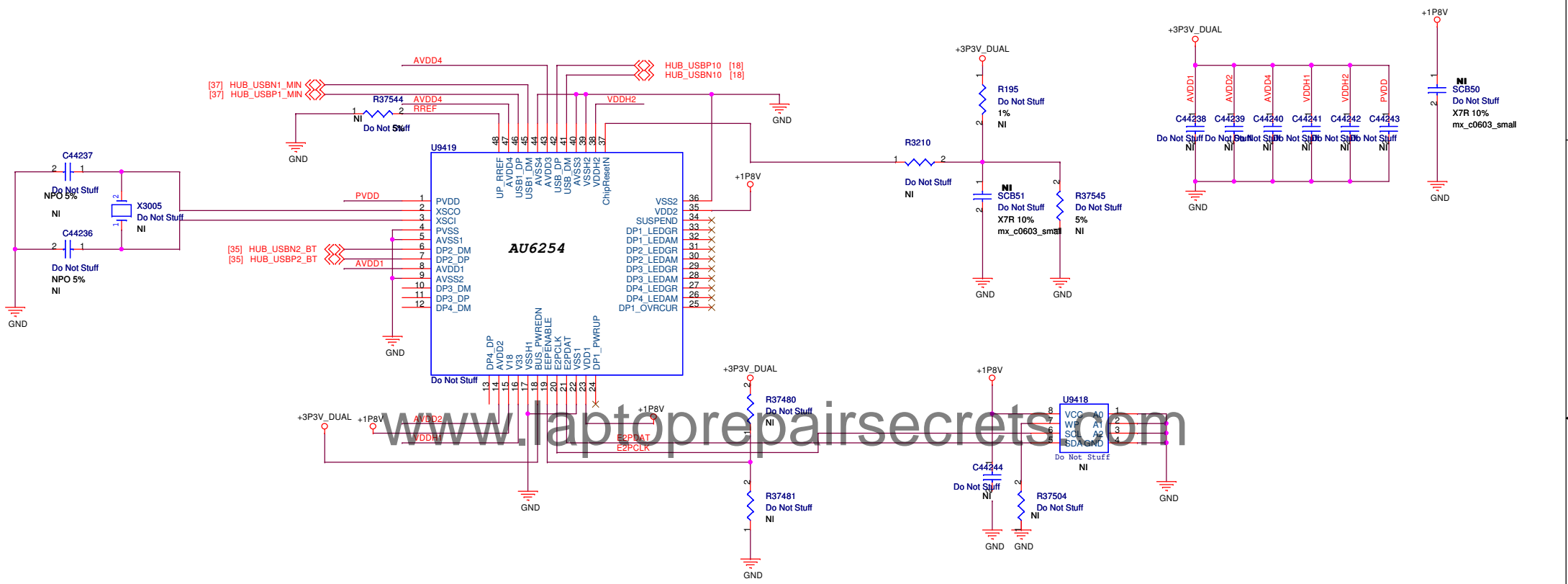
emi指定位置



EMI修改

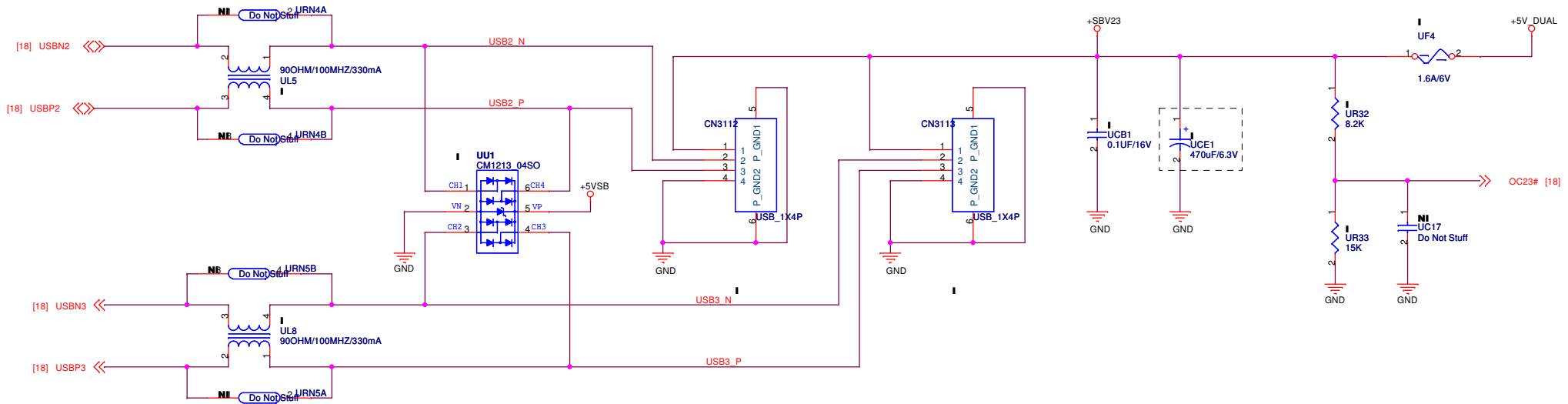
EMI修改



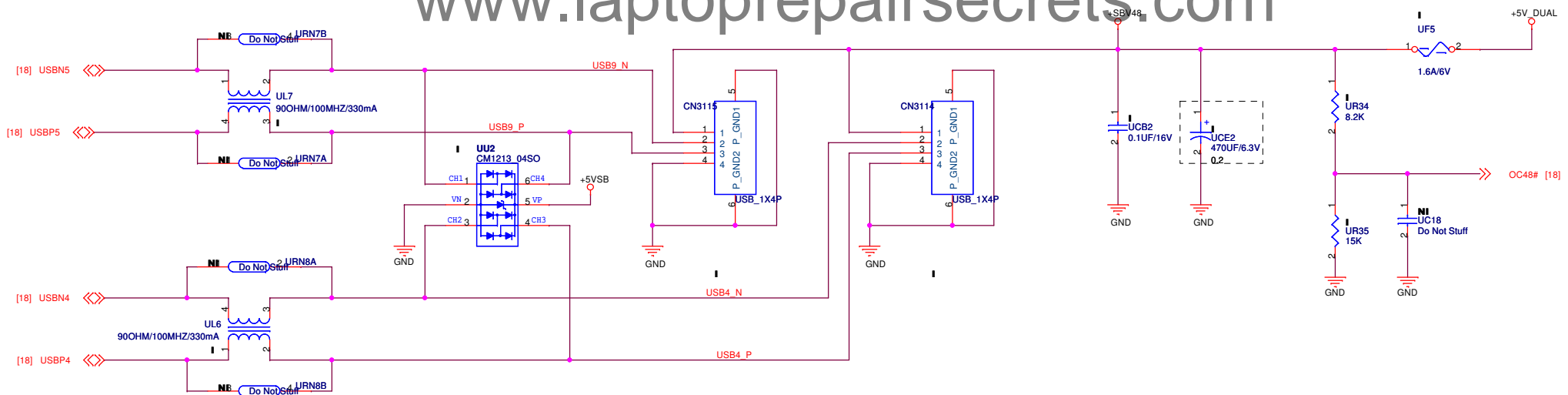


整頁修改過

Rear USB2.0 *4

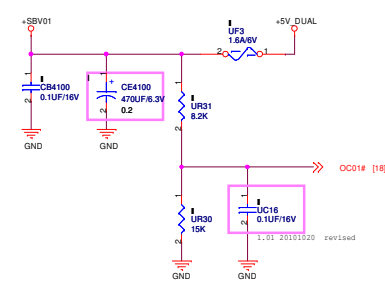
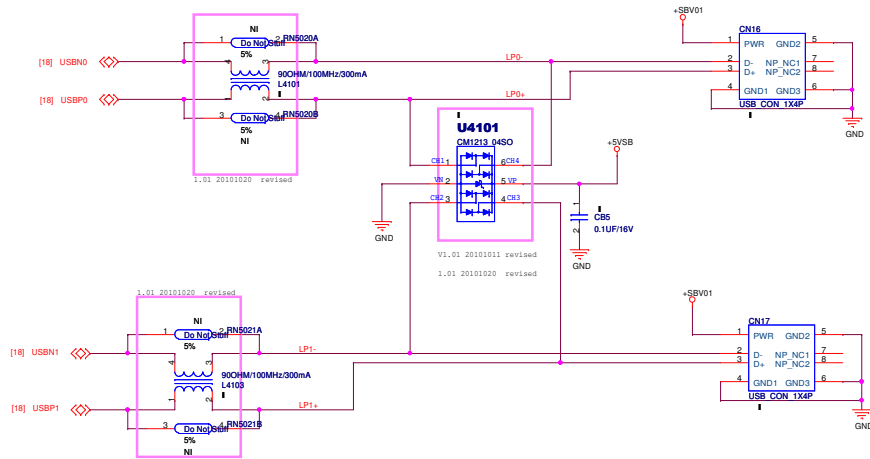


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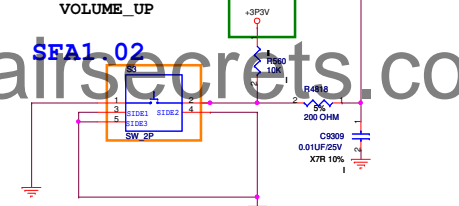
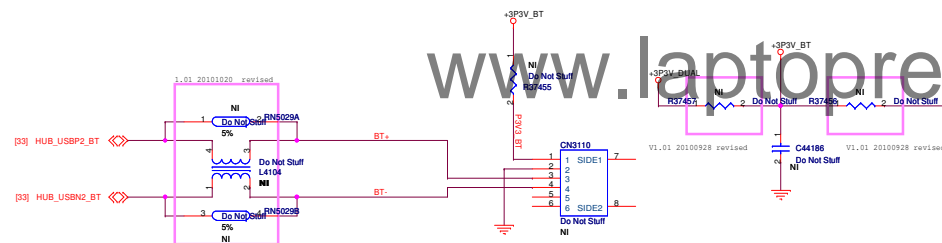
Side USB

已修改過

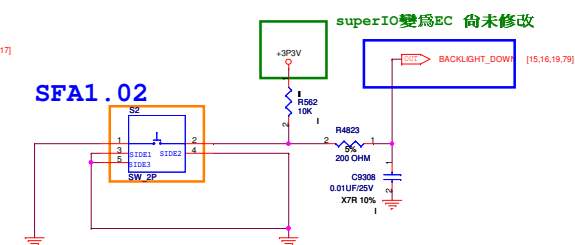
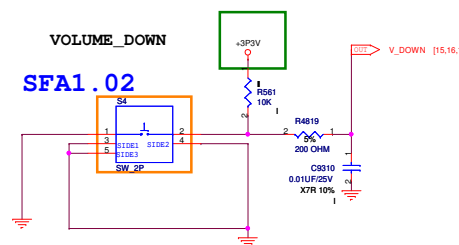
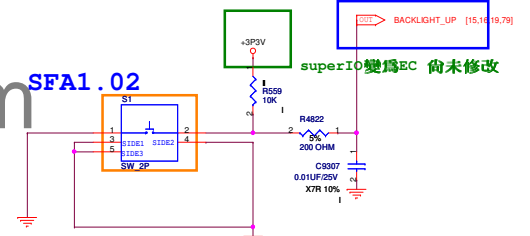


另外增加
Internal I/O
BLUE TOOTH

the DMC device connected BT symbols is needed

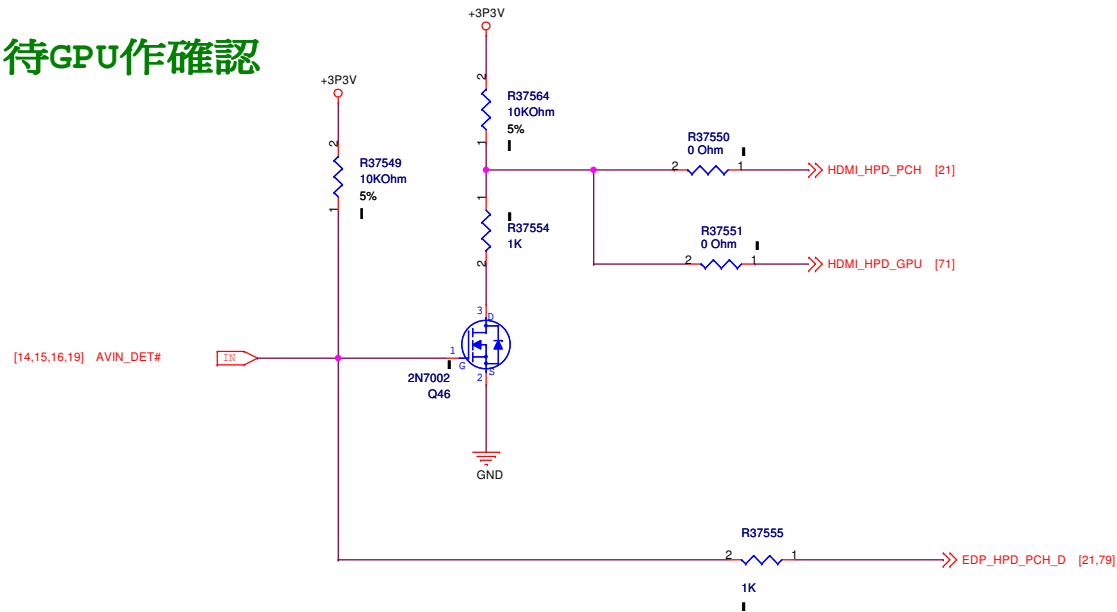


CTRL VOLUME

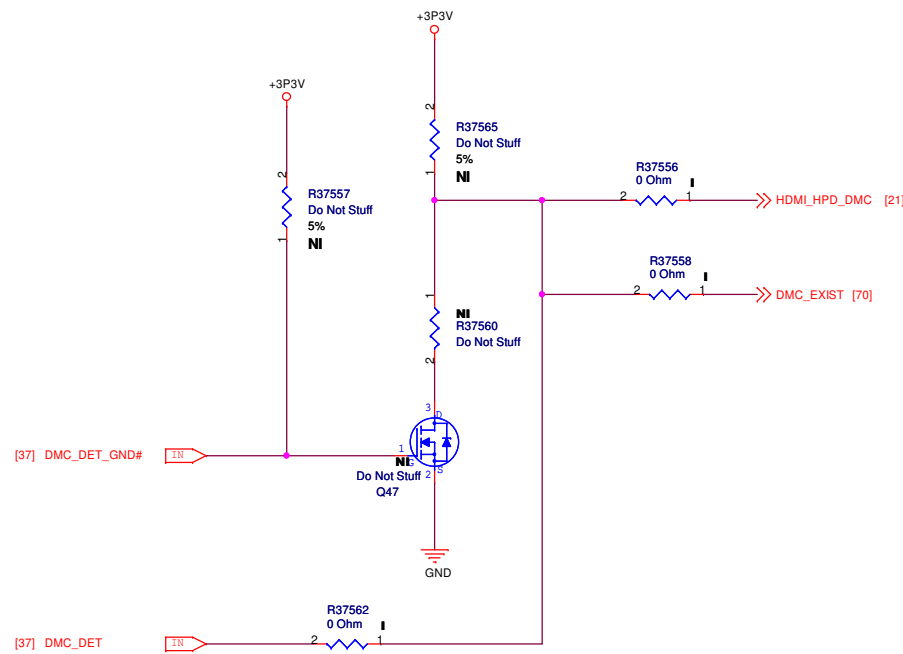


0413

待GPU作確認

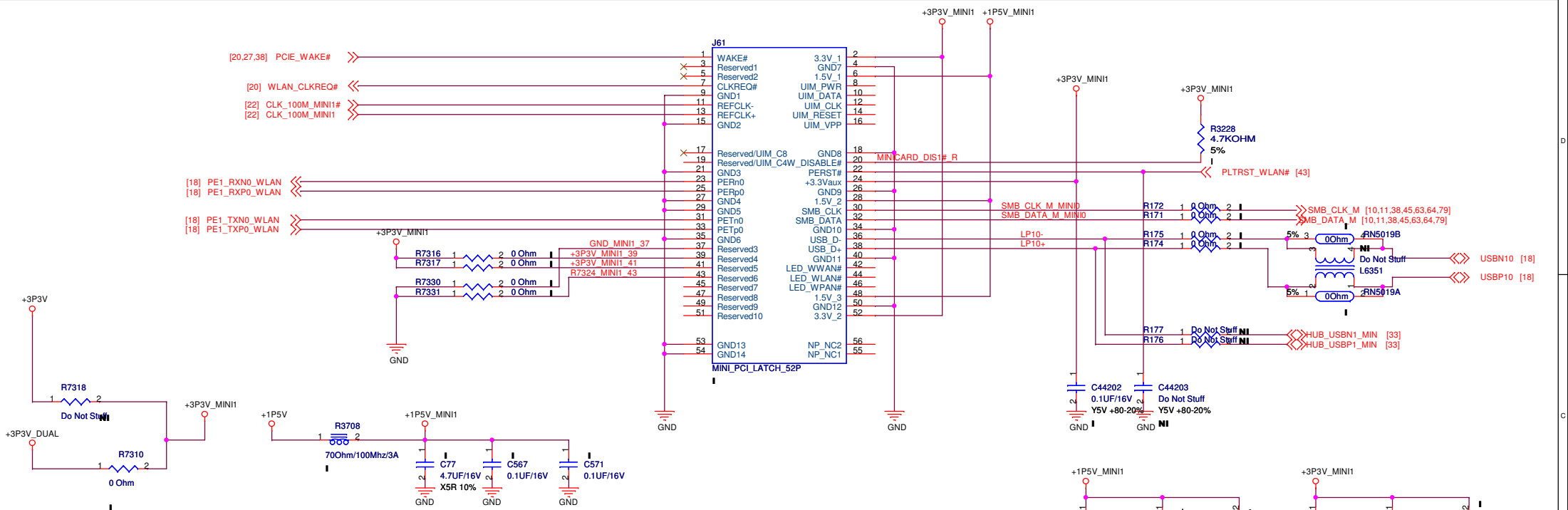


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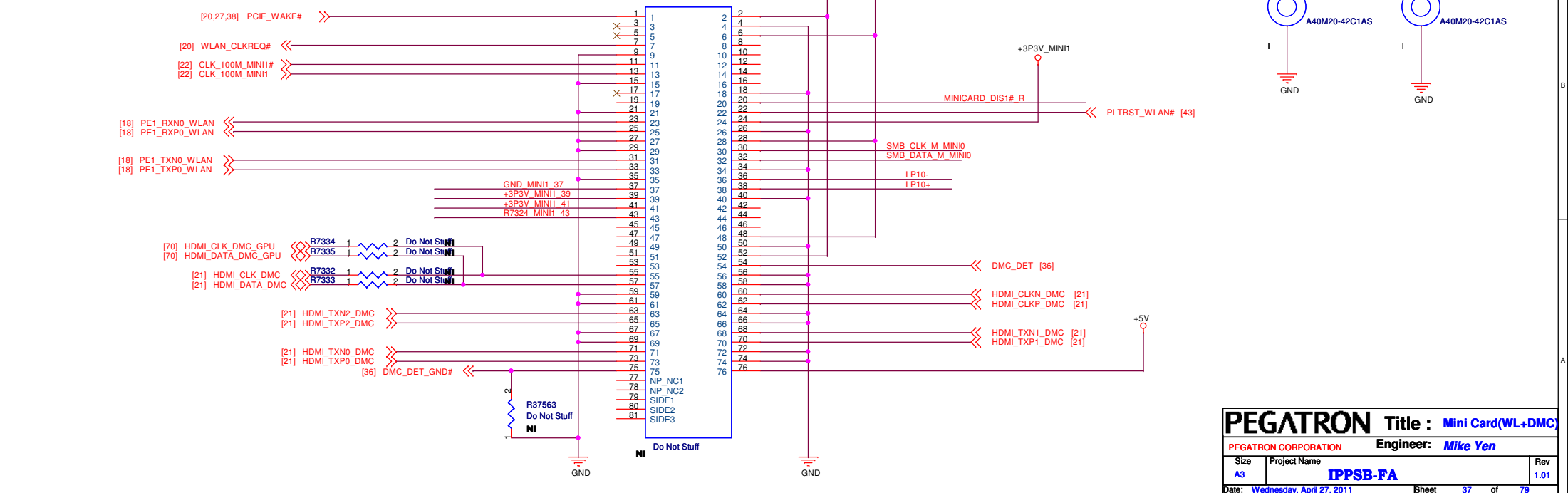
0413

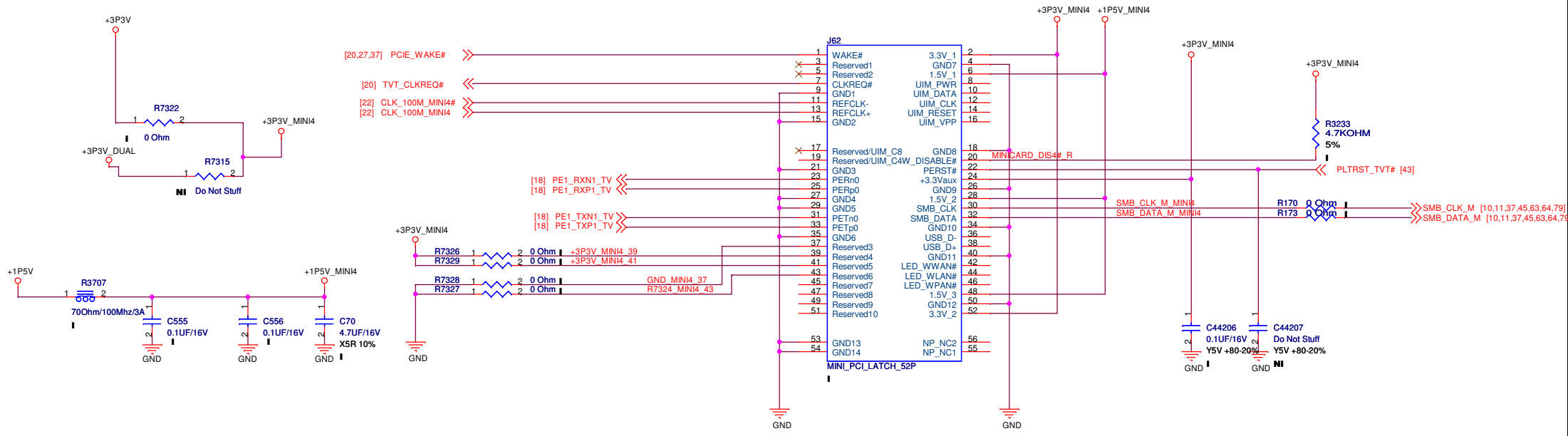
| | | | |
|--|---------------------------------|-------------------------------|------------------------|
| PEGATRON | | Title : HPD DET | |
| R&D 2 | | Engineer: Jerry, Hsuan | |
| Size A3 | Project Name IPPSB-FA | | Rev 1.01 |
| Date: Wednesday, April 27, 2011 | | Sheet | 36 of 79 |



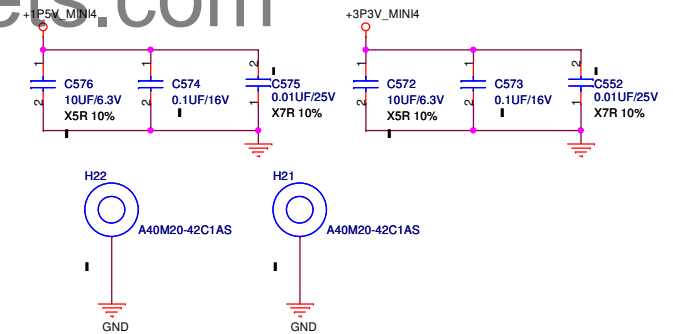
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CON5134上件時 周邊元件也需上件





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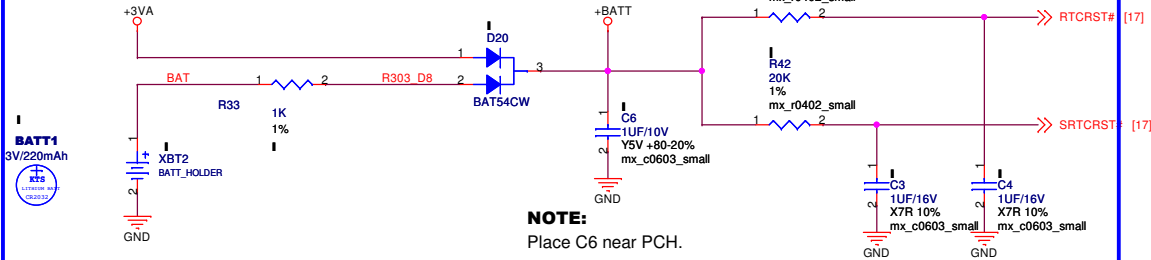
0413

CLR CMOS CIRCUIT

CLR PASSWORD CIRCUIT

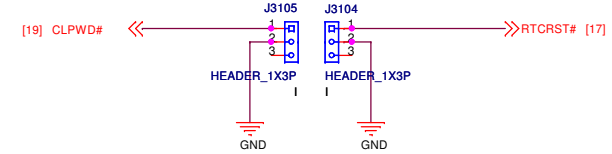
更換SCOTT的

External RTC Circuitry



Battery Socket

| PASSWORD | |
|----------|---------|
| 1-2 | CLEAR |
| 2-3 | Default |

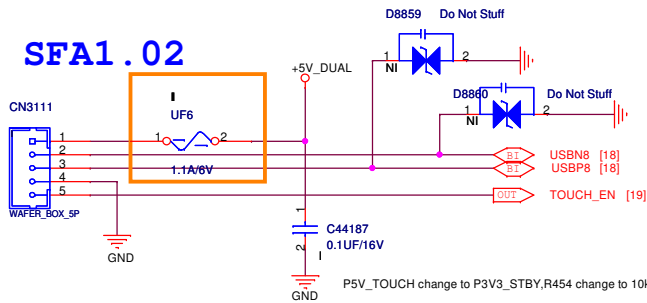


| CMOS RTC | |
|----------|---------|
| 1-2 | CLEAR |
| 2-3 | Default |

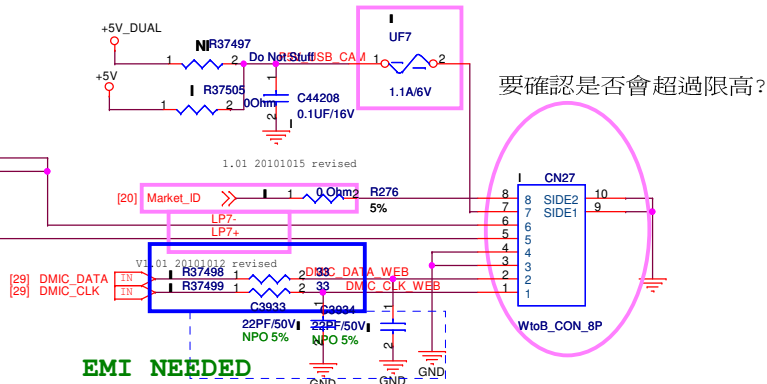


TOUCH

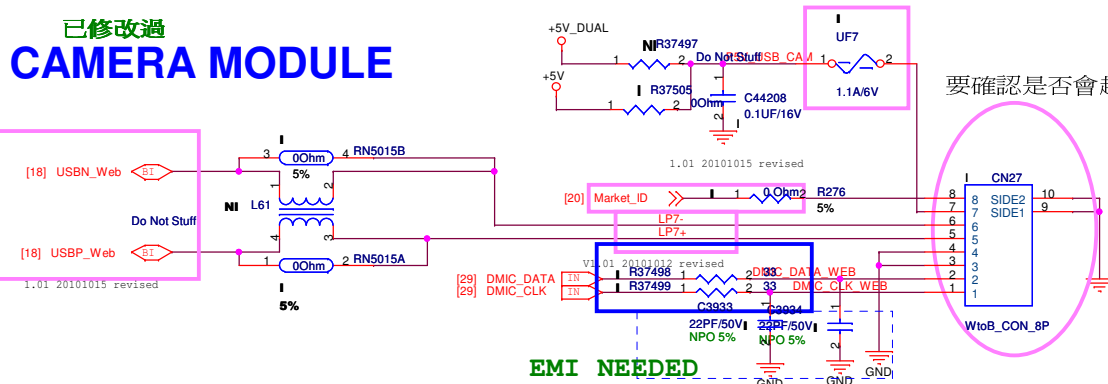
SFA1.02

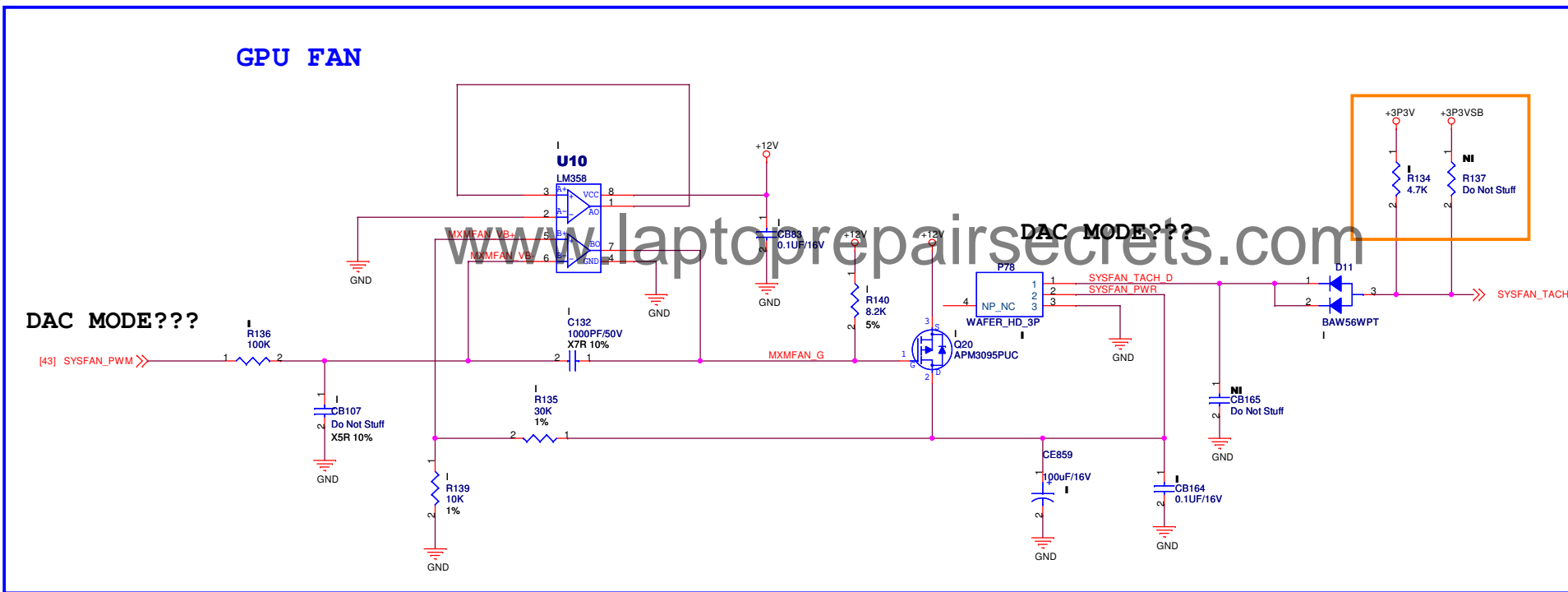
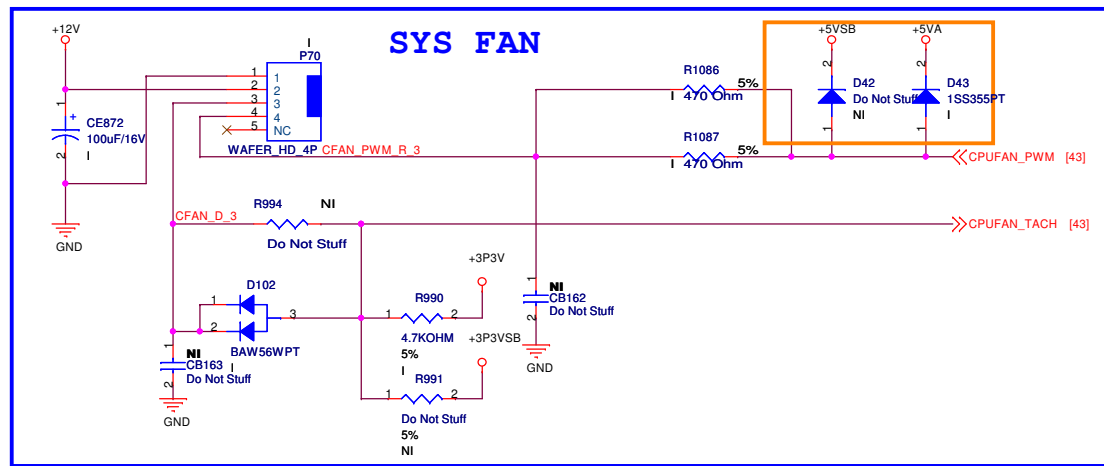


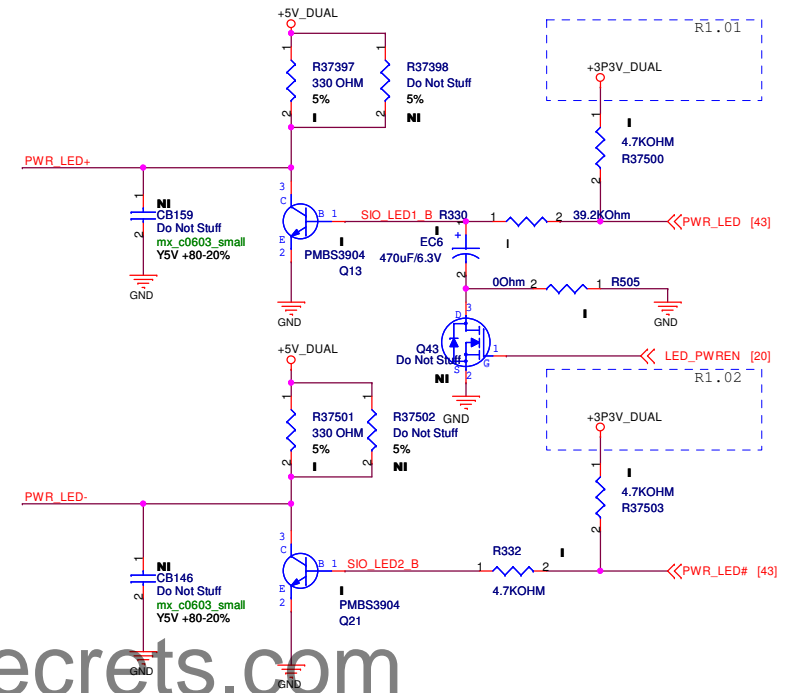
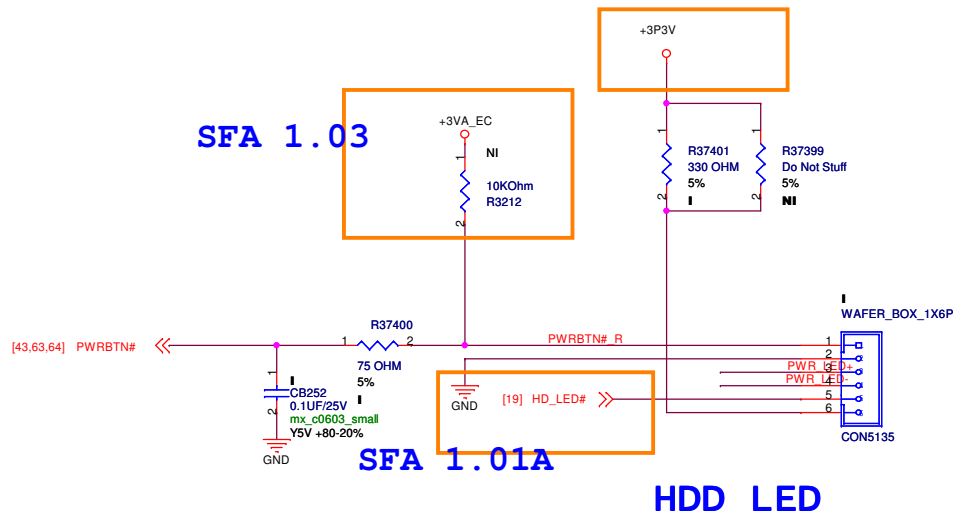
SFA1.03



已修改過 CAMERA MODULE

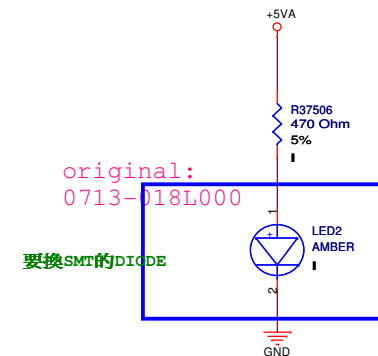






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Power supply LED

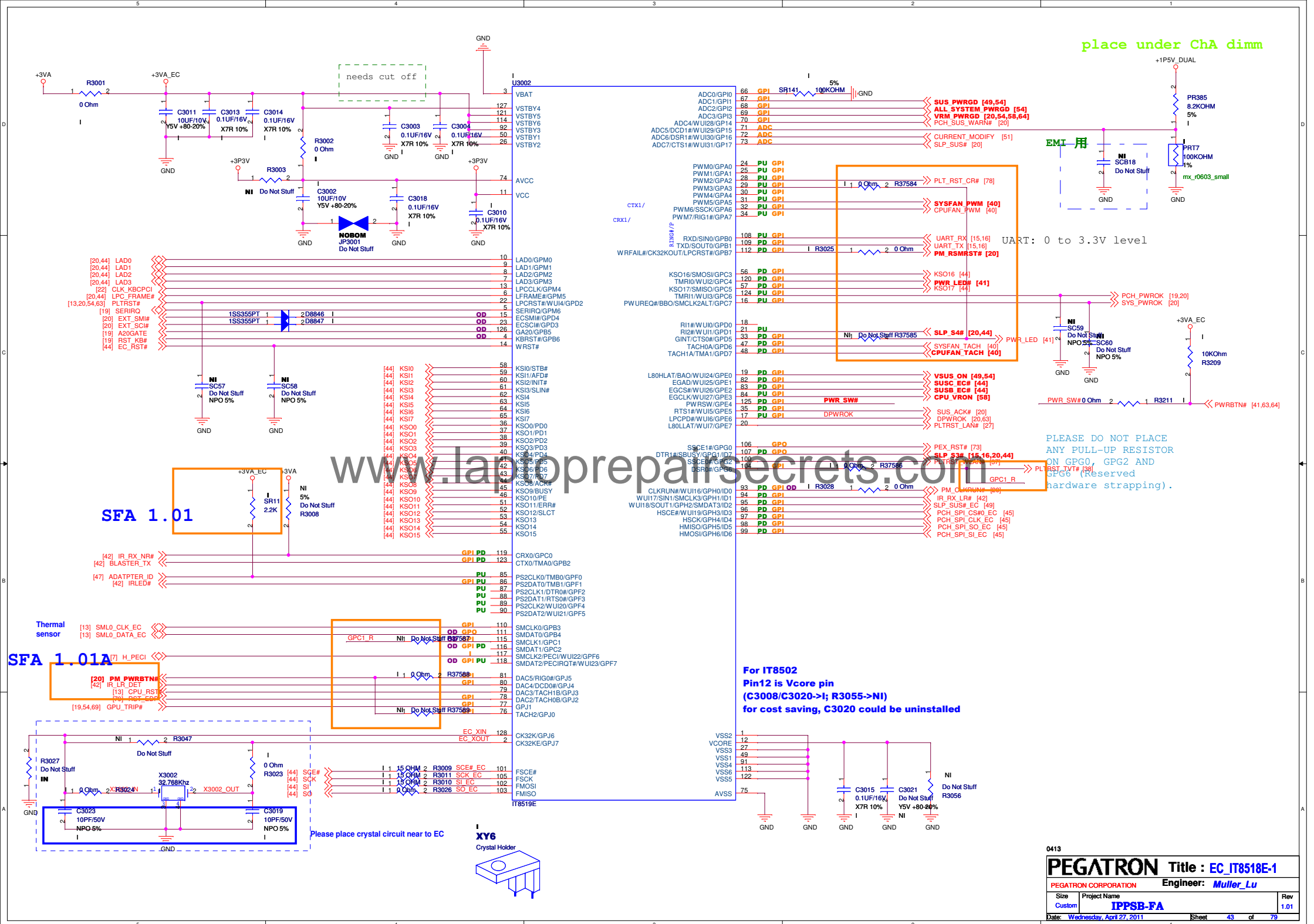


IR Blaster

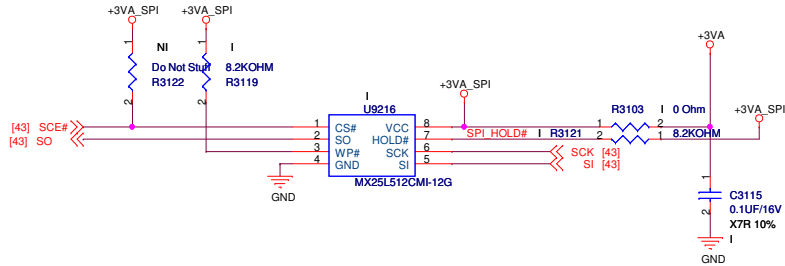


IR 已修改完成





SPI ROM+ External programming conn.

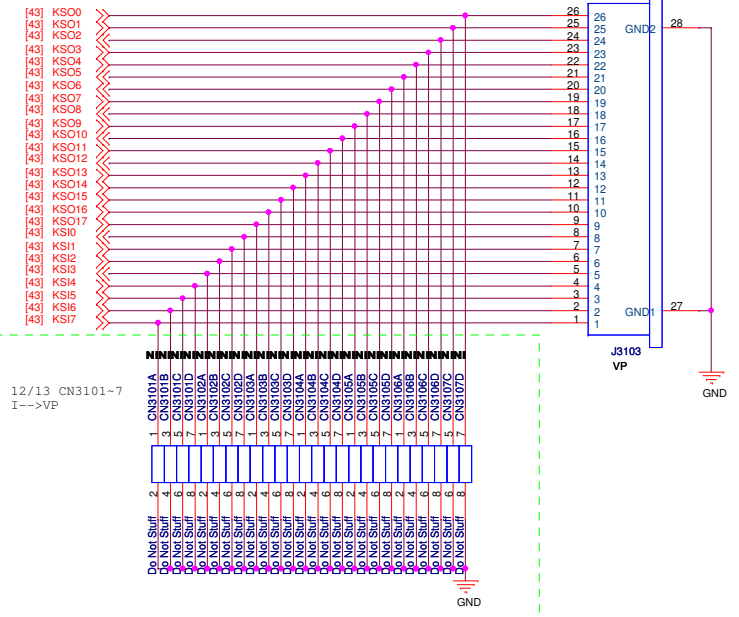


Touch PAD(deleted)

For Instant Key & Switch

Note: Close to EC

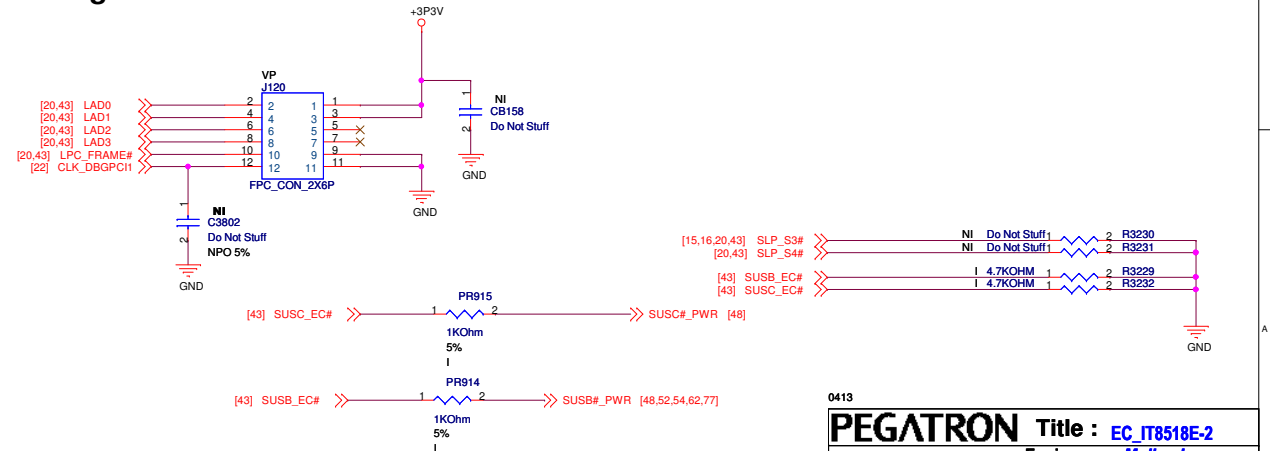
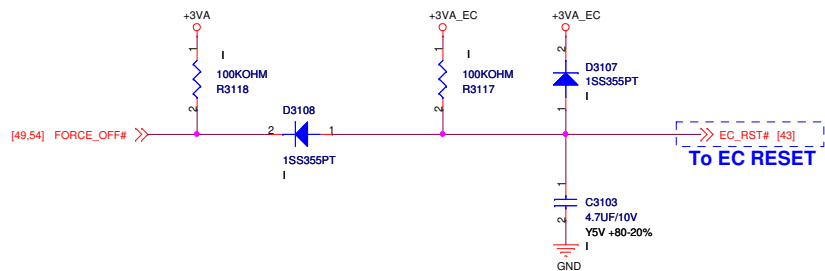
Keyboard Connector(debug)



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For EC PU/PD

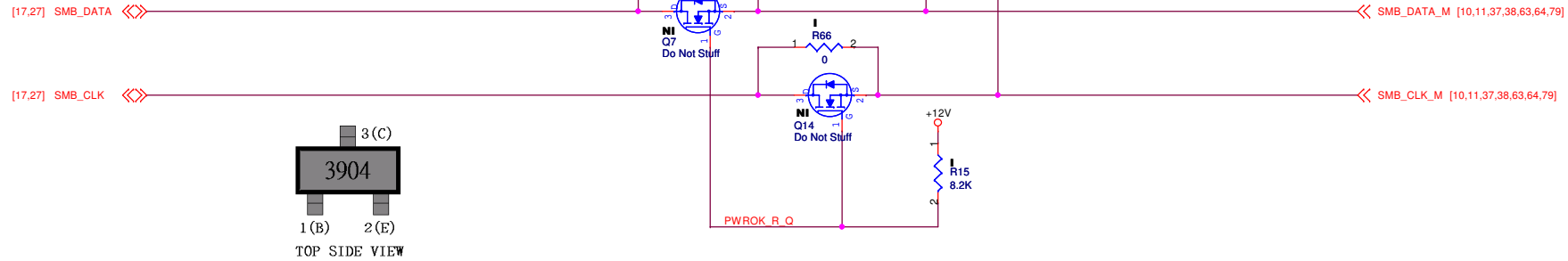
Debug Card CON



0413

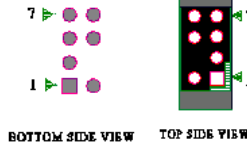
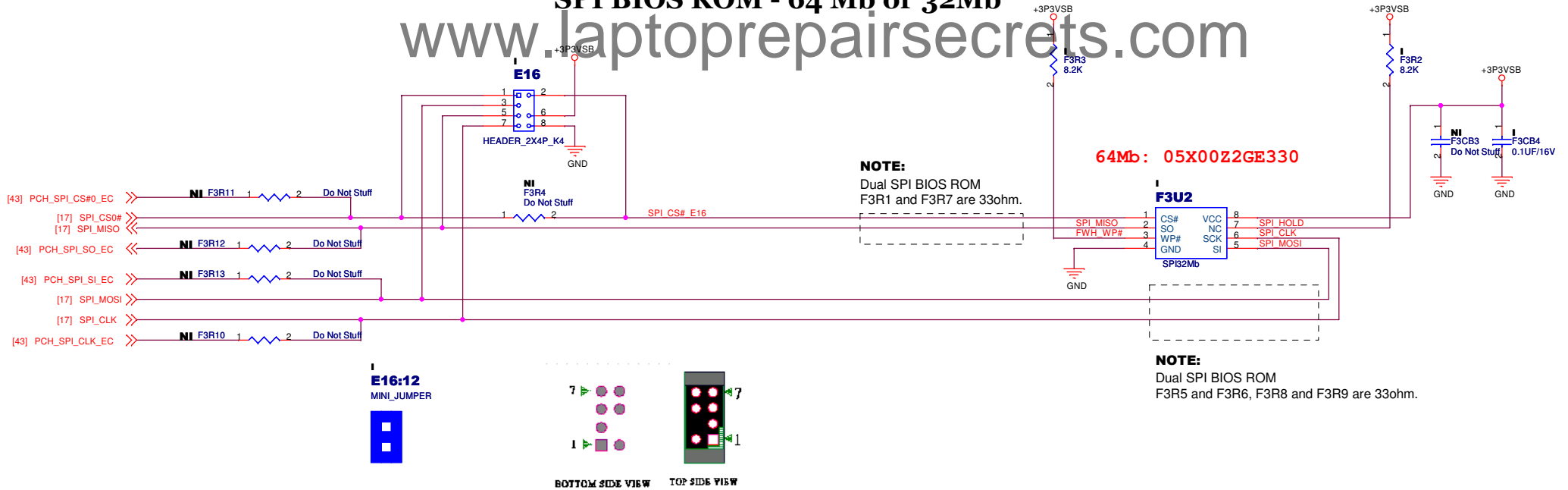
SM BUS Control

To PCH, PCI, and PCIE Slot



SPI BIOS ROM - 64 Mb or 32Mb

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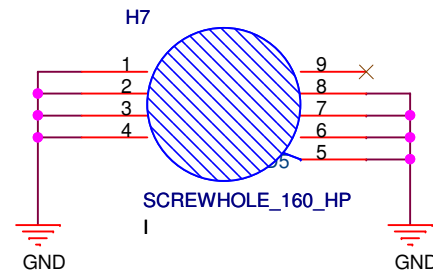
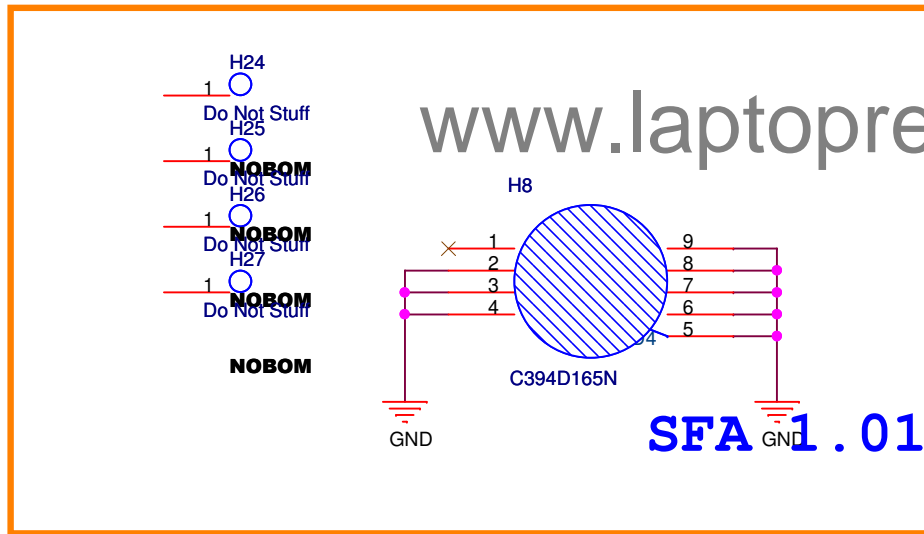
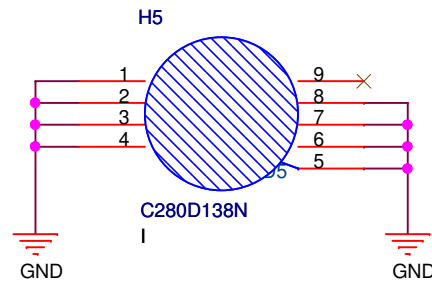
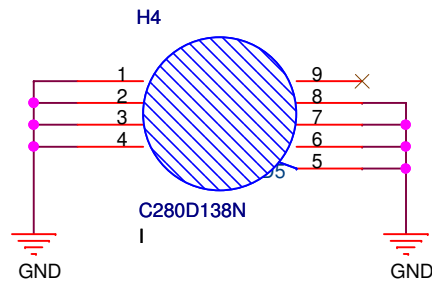
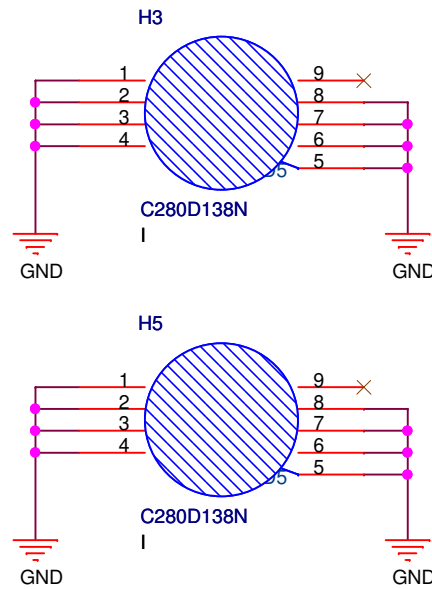
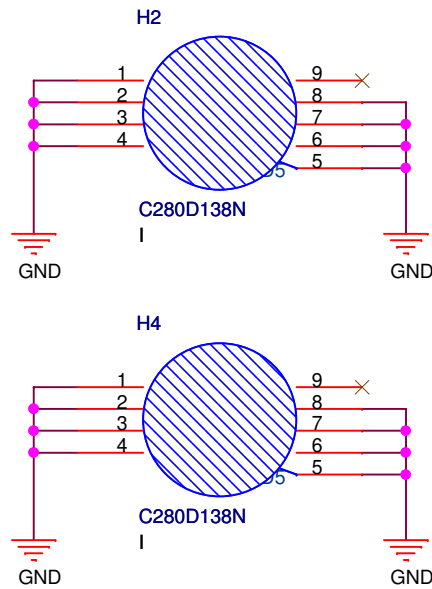
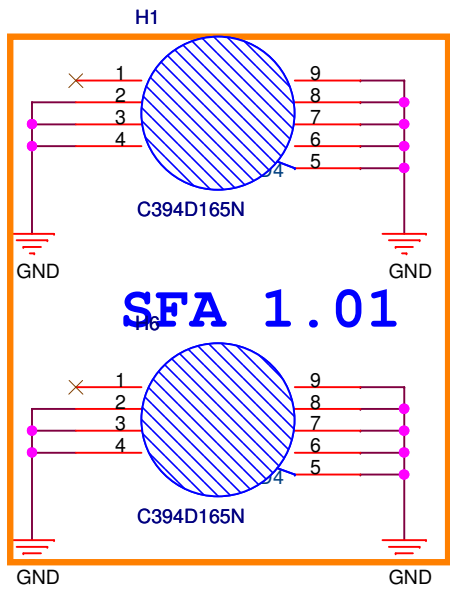
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SM BUS & SPI ROM

PEGATRON CORPORATION Engineer: XXXX-XX

Size A3 Project Name IPPSB-FA Rev 1.01

Date: Wednesday, April 27, 2011 Sheet 45 of 79

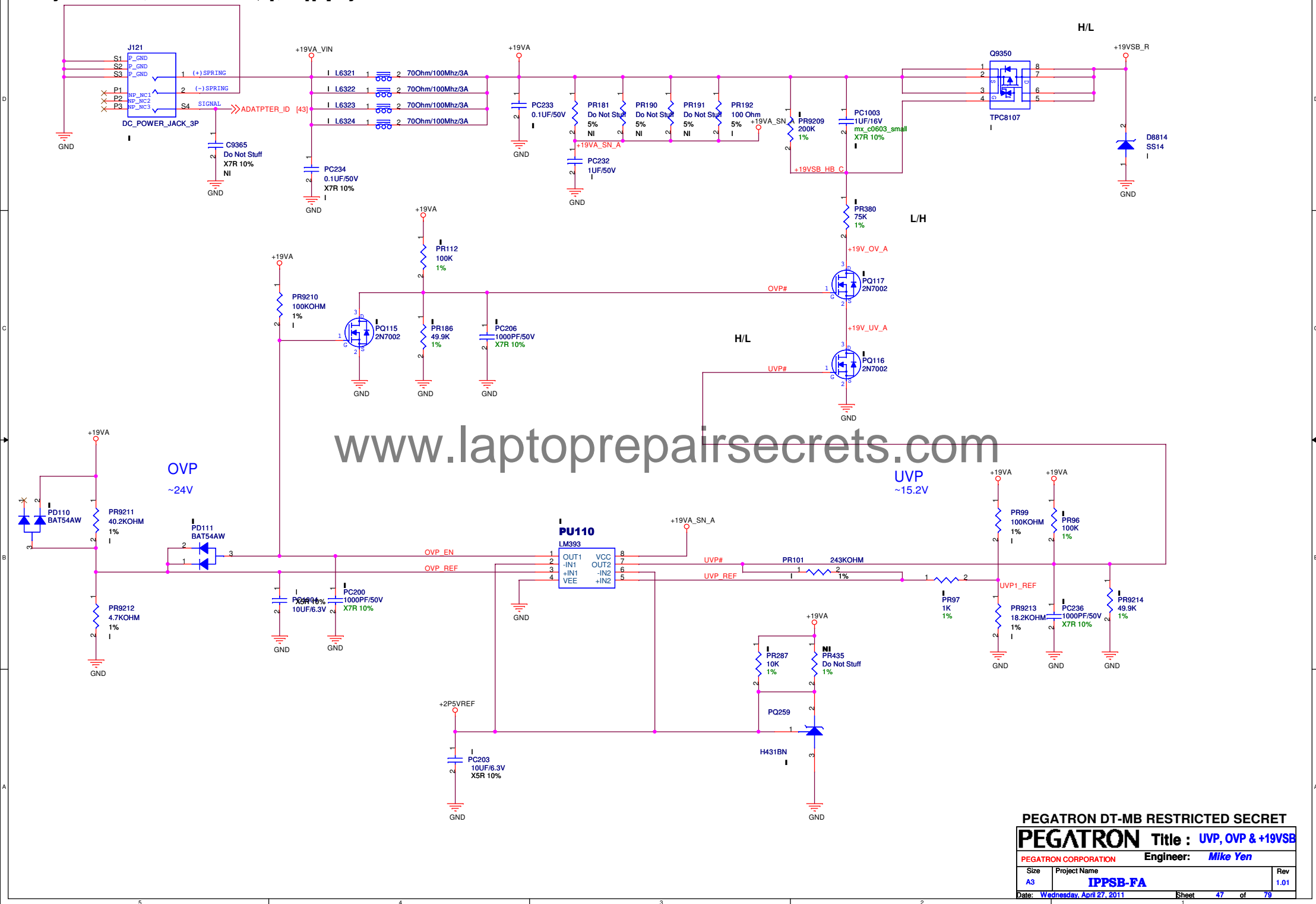


VESA mount hole

0413

| | | |
|--|---------------------------------|------------------------------|
| PEGATRON | | Title : SCREW HOLE |
| PEGATRON CORPORATION | | Engineer: Mike Yen |
| Size A | Project Name IPPSB-FA | Rev 1.01 |
| Date: Wednesday, April 27, 2011 | | Sheet 46 of 79 |

change to SIMULA /AJ261B-Y090-42F, p/n applying....



+19VSB
lin=5.95A
Trace Width>240mil

+5VSB
I_{max}=18.07A
TDC=12.65A
Trace Width>730mil

+19VSB
lin=3.25A
Trace Width>130mil

+3P3VSB
Imax=16.63A
TDC=11.65A
Trace Width>680mil

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```
OCP :
+5VSB : 21.0A
+3P3VSB : 20.1A

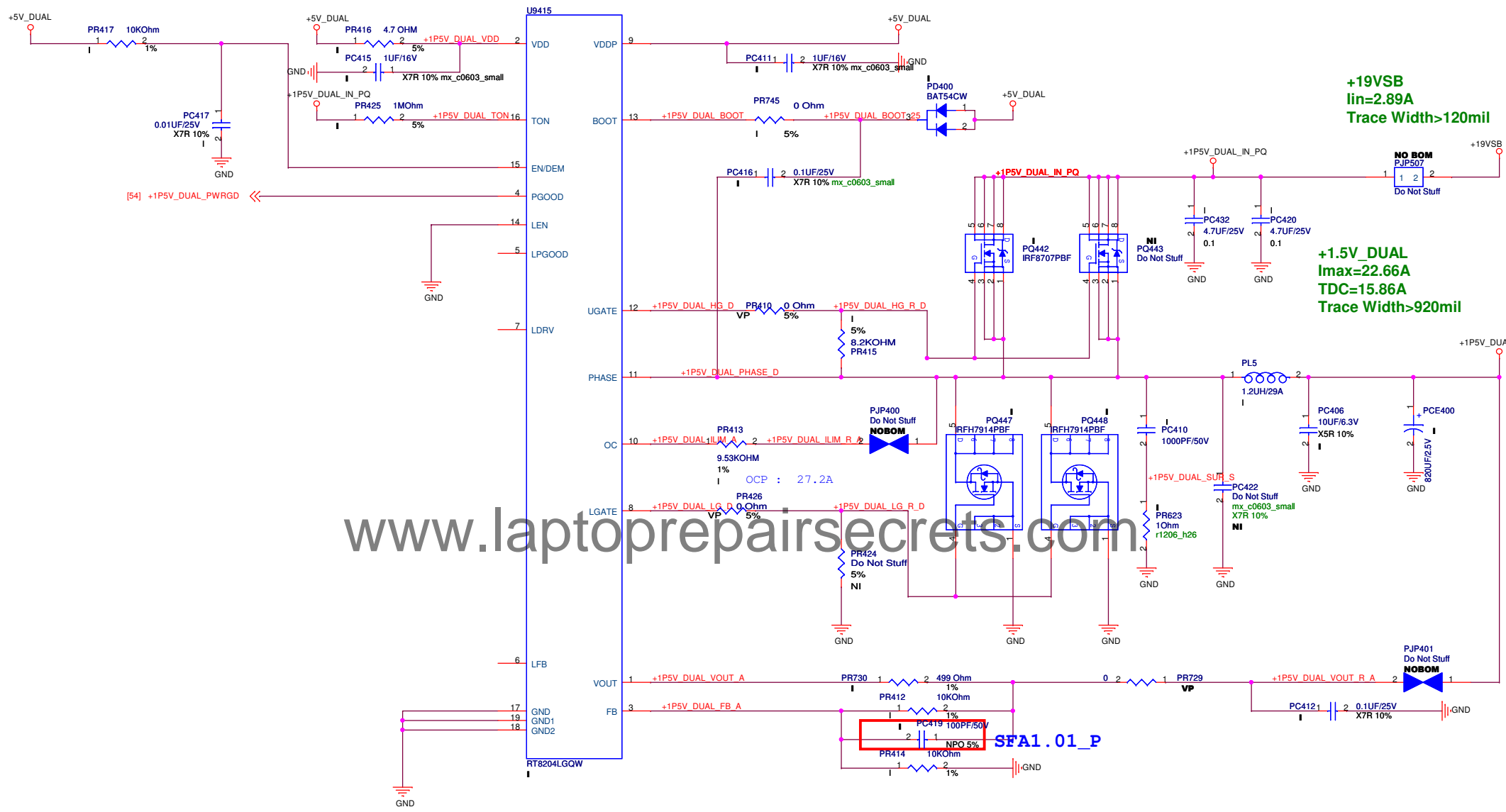
FSW :
+5VSB : 245kHz
+3P3VSB : 305kHz
```

PEGATRON Title : +3VA&+3VSB&+5VSB

PEGATRON CORPORATION Engineer: **Mike Yen**

| Size | Project Name | Rev |
|------|--------------|-----|
|------|--------------|-----|

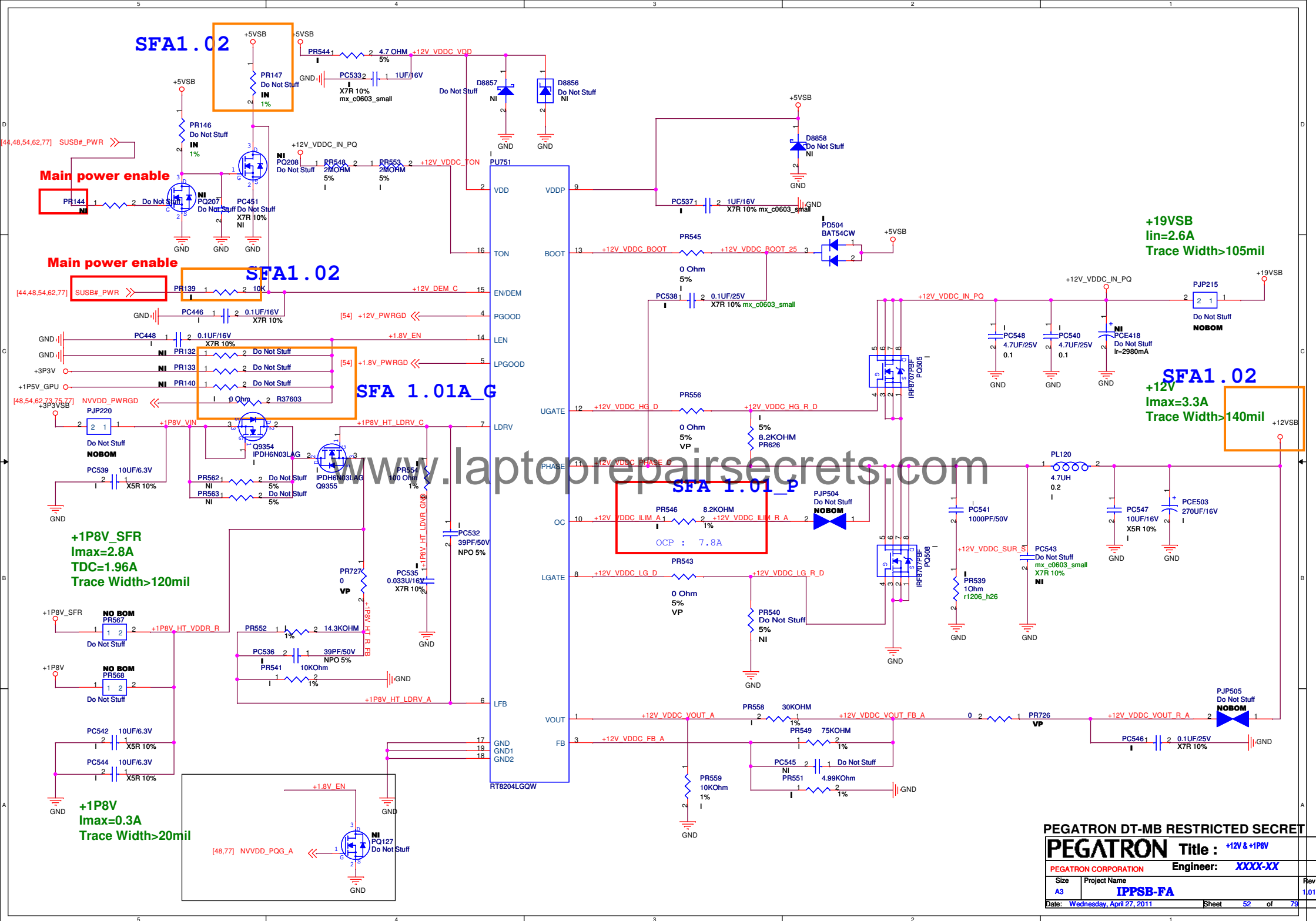
| | | |
|--------|-----------------|------|
| Custom | IPPSB-FA | 1.01 |
|--------|-----------------|------|



+19VSB
lin=2.89A
Trace Width>120mil

+1.5V_DUAL
Imax=22.66A
TDC=15.86A
Trace Width>920mil

SFA1.01_P



SFA1.01

SFA1.01

SFA1.01_P

SFA1.01_P

SFA1.01_P

+19VSB
lin=1.26A
Trace Width>50mil

+1P05V_CPUIO
Imax=18.3A
TDC=12.81A
Trace Width>720mil

+0P925V_SA
Imax=8.8A
TDC=6.16A

From CPU

From CPU

| VCCSA_VID | +0P925V_SA |
|-----------|------------|
| 0 | 0.925V |
| 1 | 0.85V |

| VCCIO_SEL | +1P05V_CPUIO |
|-----------|--------------|
| 0 | 1.00V |
| 1 | 1.05V |

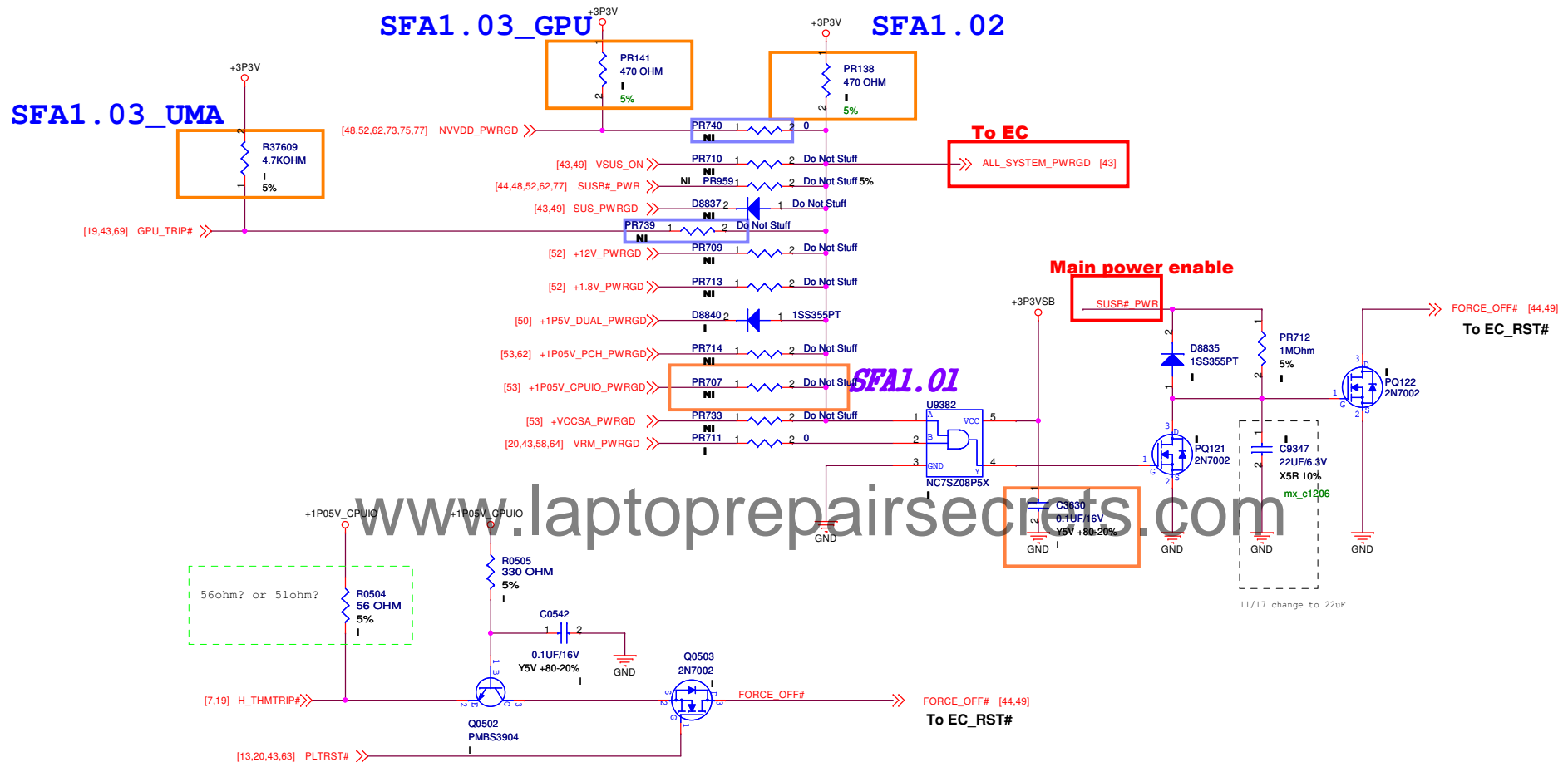
PEGATRON DT-MB RESTRICTED SECRET

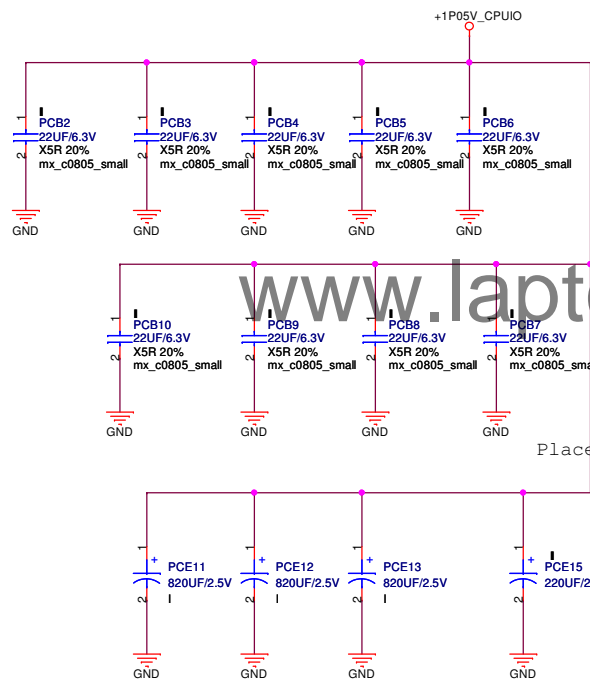
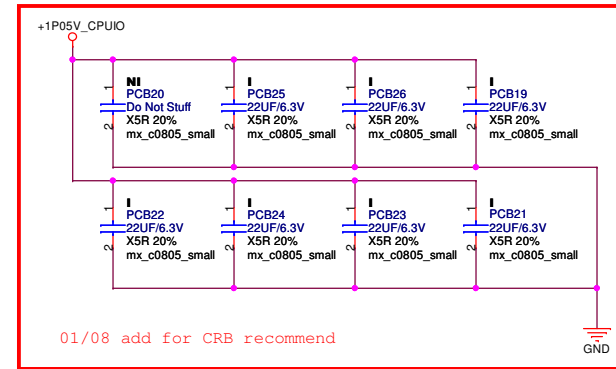
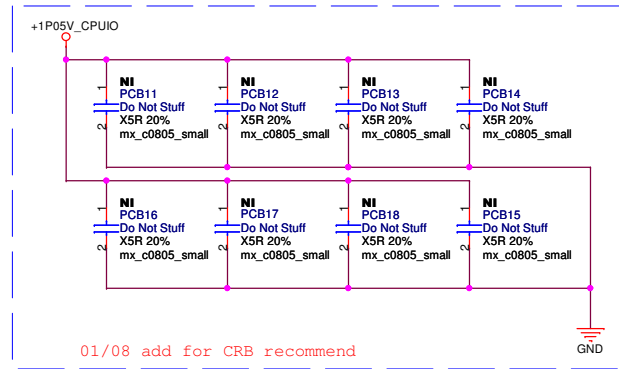
PEGATRON Title : **+1P05V_CPUIO CONTROLLER**

PEGATRON CORPORATION Engineer: **XXXX-XX**

Size A3 Project Name **IPPSB-FA** Rev 1.01

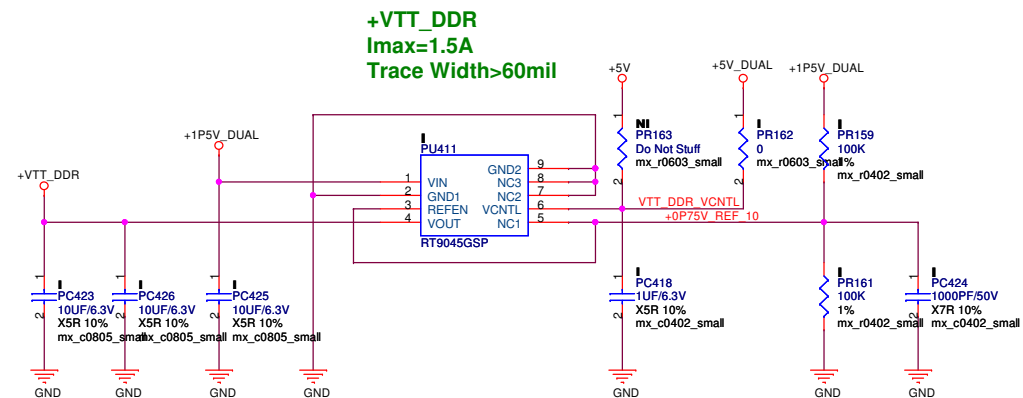
Date: Wednesday, April 27, 2011 Sheet 53 of 79



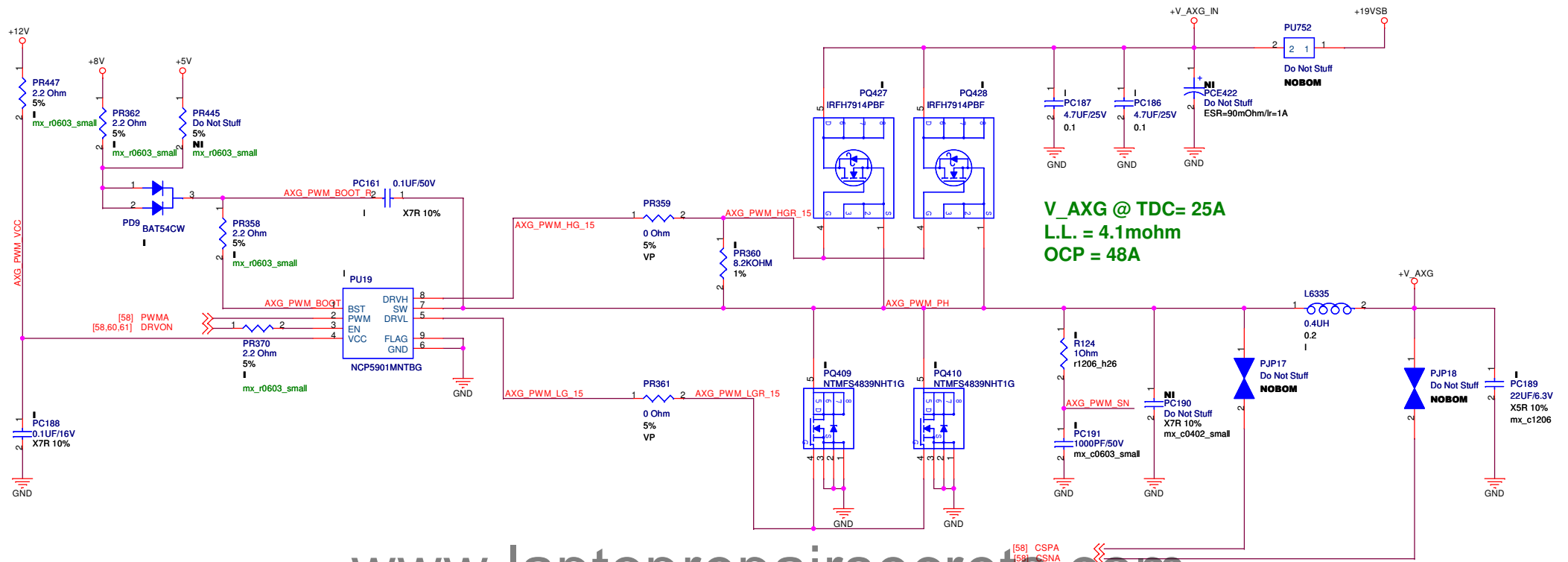


VCCIO Decoupling Requirements

| Capacitance | Qty | ESR (each) | ESL (each) | Filter | Placement | Notes |
|------------------------|-----|------------|------------|--------|--------------------------------|---------|
| Aluminum Polymer 560μF | 3 | 7mΩ | 1.4nH | Output | Various. See layout figures | 1 |
| 22μF 0805 X5R | 9 | 5mΩ | 0.55nH | Output | Inside processor socket cavity | 1, 2, 3 |
| 0805 padholders | 16 | | | | Backside | |



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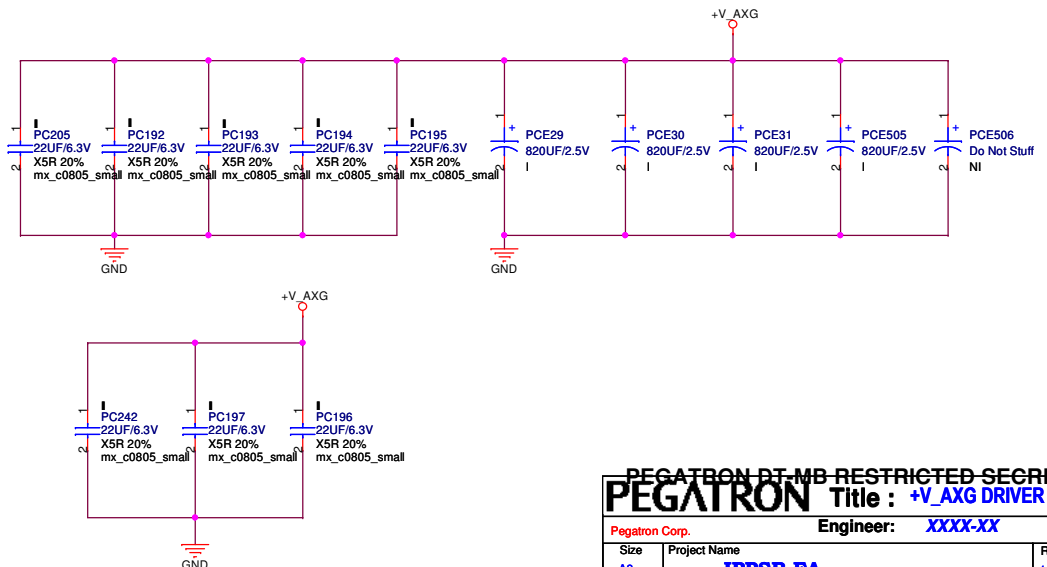
www.laptoprepairsecrets.com

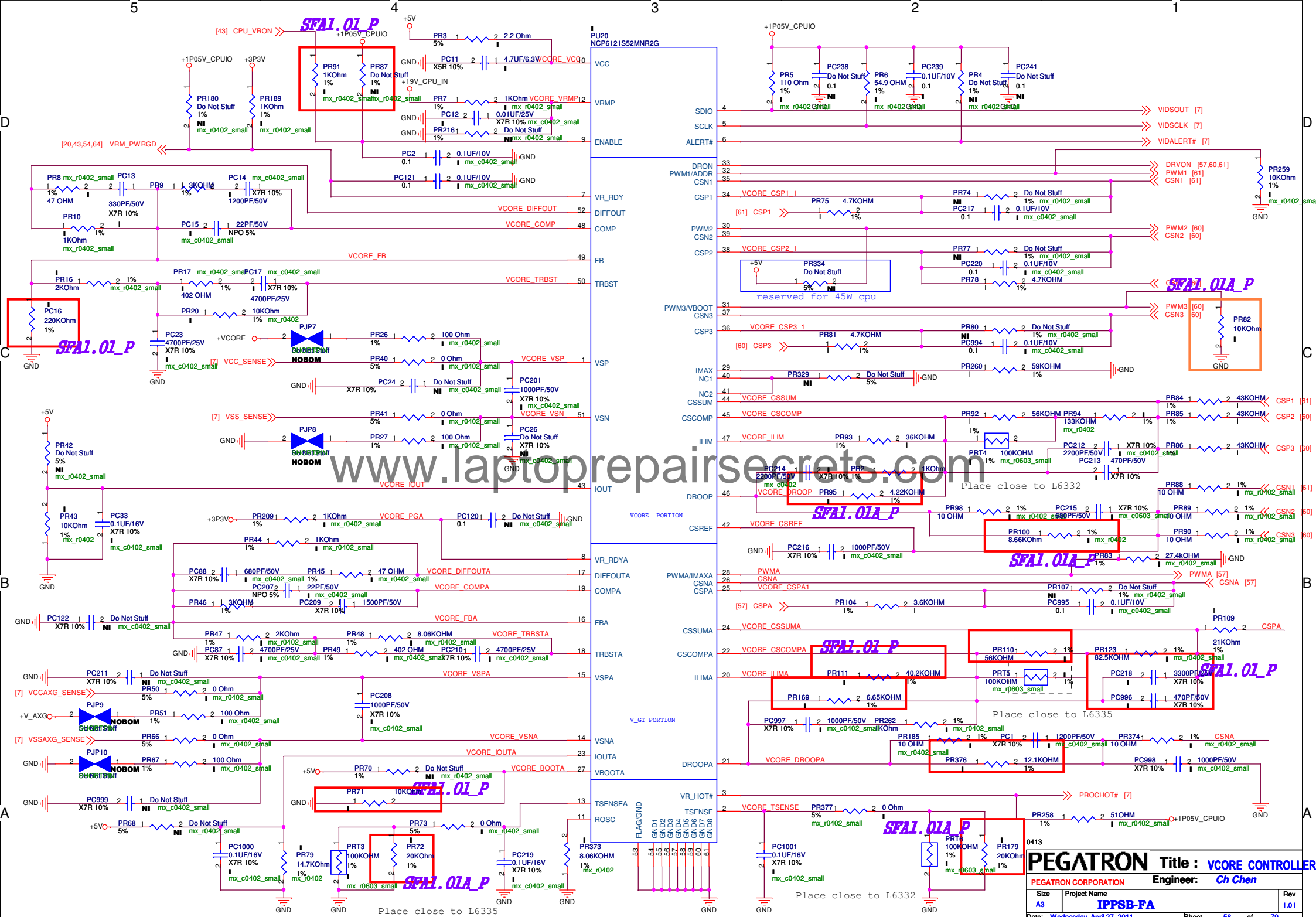
Output CAP

Table 30-4. VCCAXG Decoupling Requirements

| Capacitance | Qty | ESR (each) | ESL (each) | Filter | Placement | Notes |
|------------------------|-----|------------|------------|--------|---|--------|
| Aluminum Polymer 560µF | 4 | 7mΩ | 1.4nH | Output | East of processor - as close to RM keep-out as possible | 1 |
| 22µF 0805 X5R | 6 | 5mΩ | 0.55nH | Output | 4 - inside processor socket cavity 2(empty) - Bottom of board, near socket | 1, 2 3 |
| 4.7µF X5R | 3 | 7mΩ | 0.6nH | Input | | 1 |

PL-CAP *4
MLCC *6



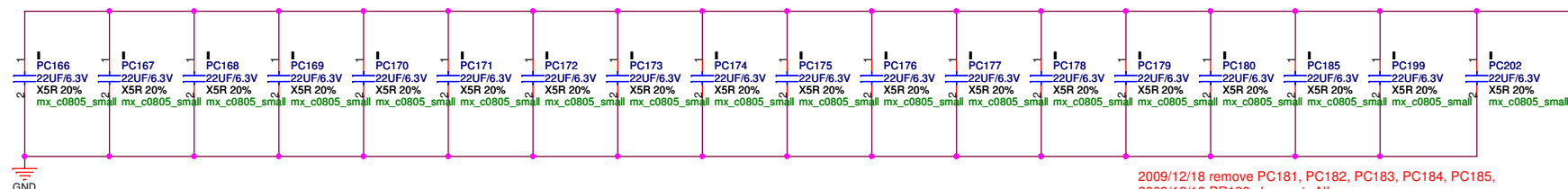
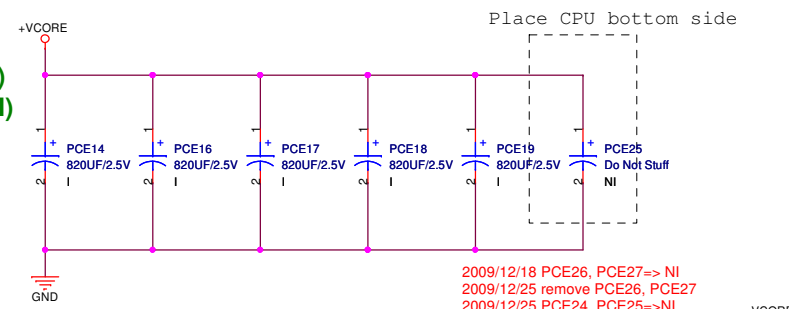


Output CAP

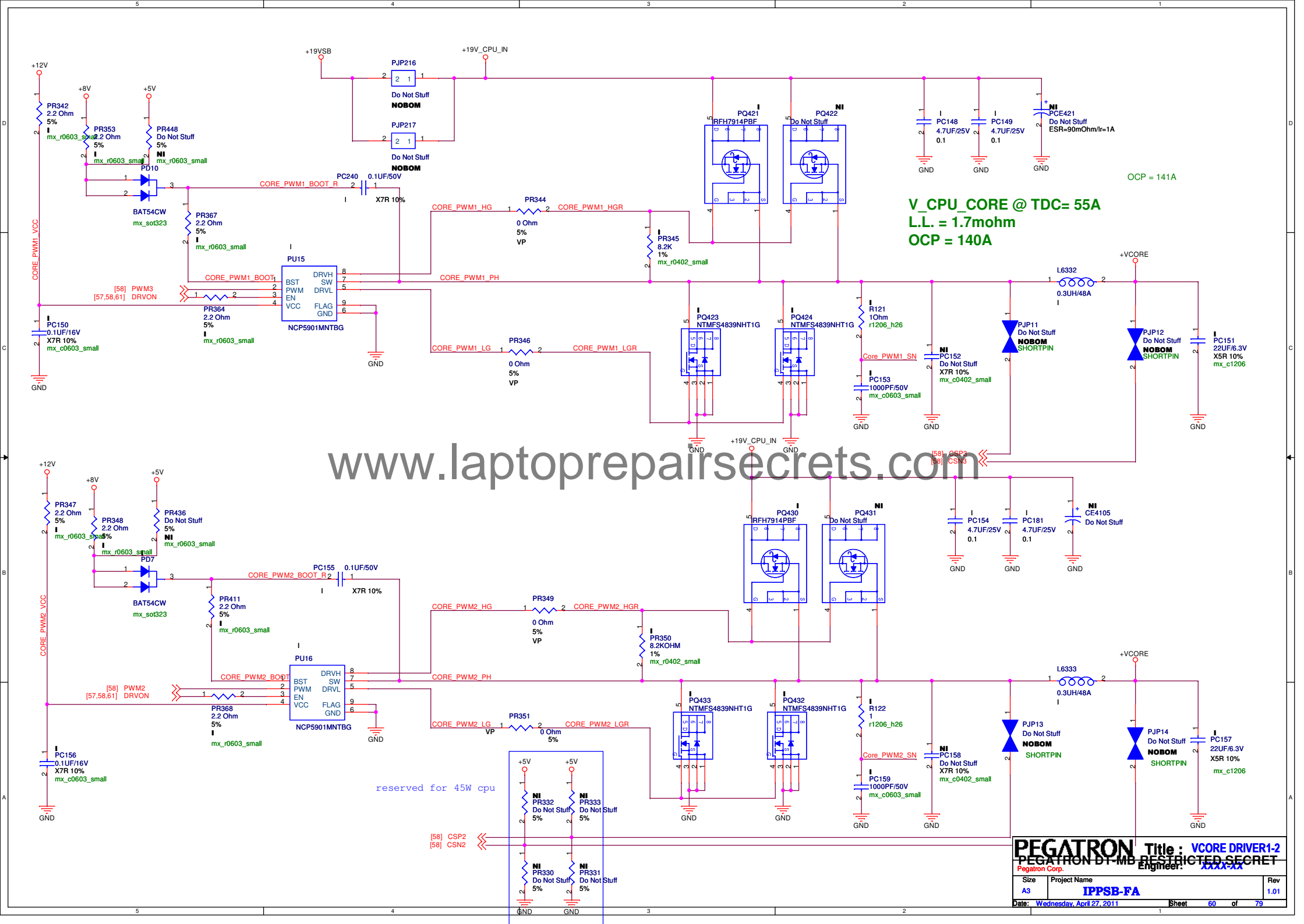
Table 30-2. Decoupling Requirements

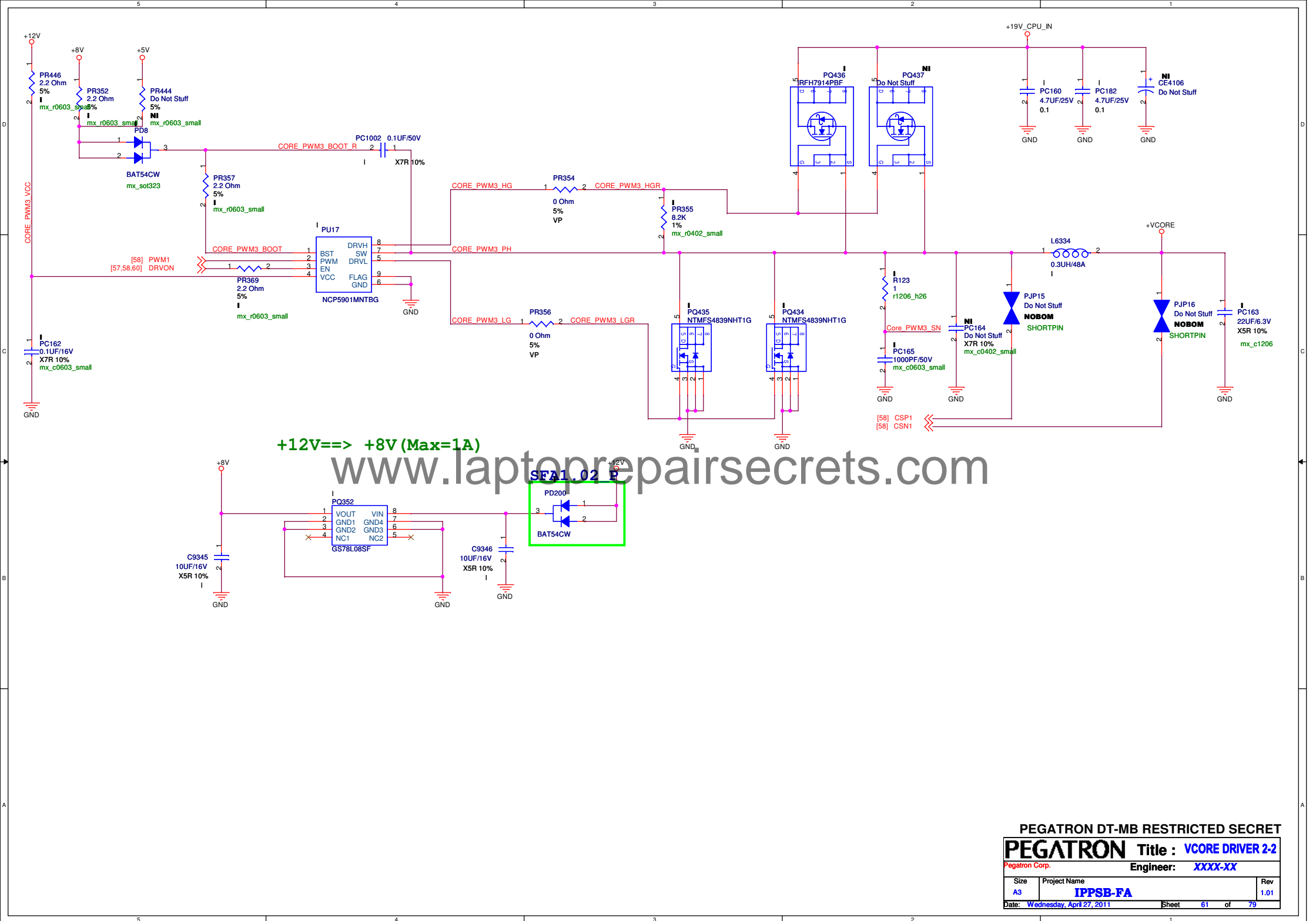
| Capacitance | Qty | ESR (each) | ESL (each) | Filter | Placement | Notes |
|-----------------------------|-----|------------|------------|--------|--|--------|
| Aluminum Polymer 560µF | 4 | 7mΩ | 1.4nH | Output | North of processor - as close to RM keep-out as possible | 1 |
| 22µF 0805 X5R | 18 | 5mΩ | 0.55nH | Output | 14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible | 1, 2 3 |
| Aluminum Electrolytic 390µF | 4 | 51mΩ | 6.1nH | Input | | 1 |
| 4.7µF X5R | 9 | 7mΩ | 0.6nH | Input | | 1 |

PL-CAP *4 +2(NI)
MLCC *18 +3(NI)



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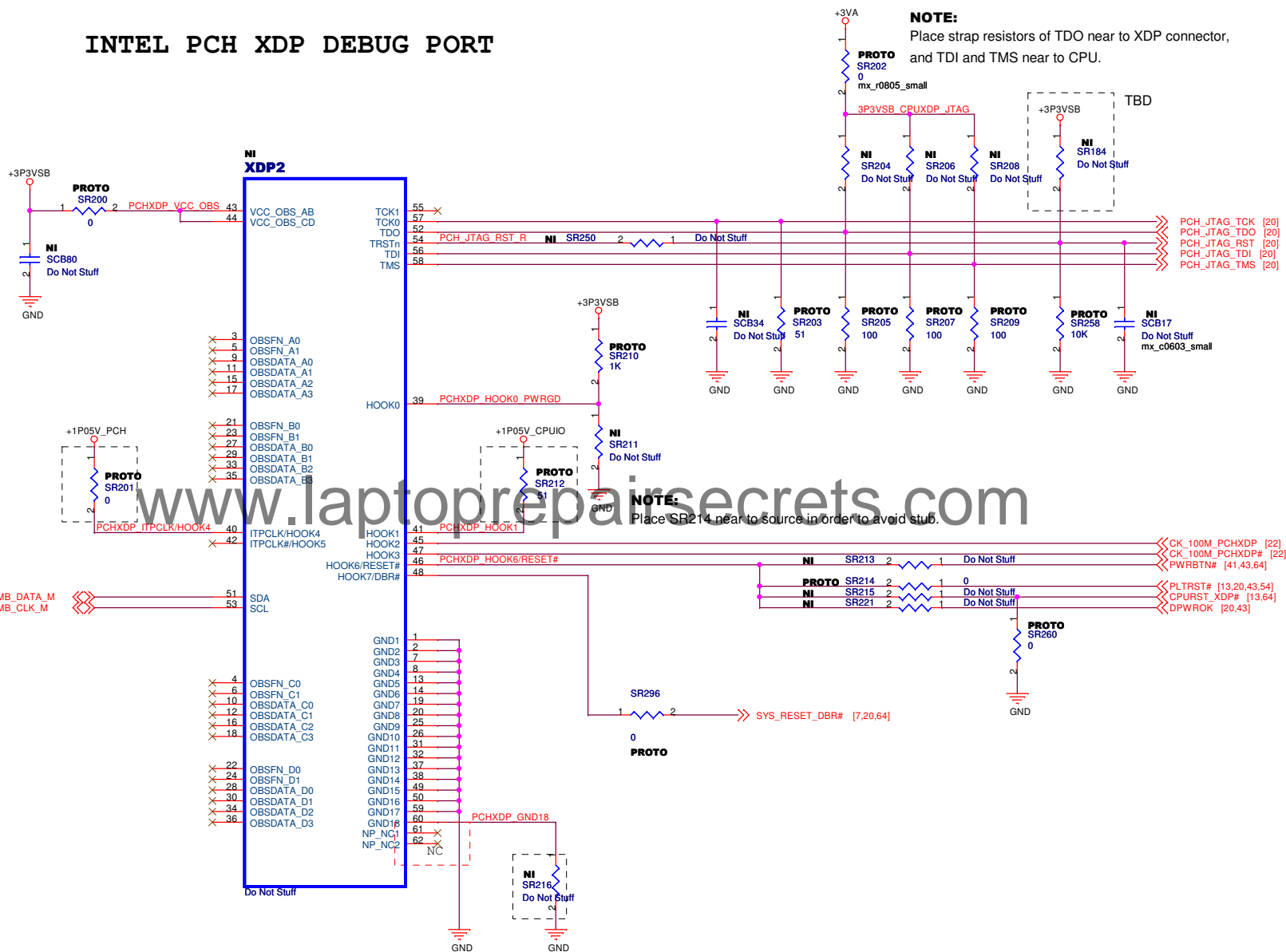






NOTE:

Place strap resistors of TDO near to XDP connector, and TDI and TMS near to CPU.



0498 REGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH XDP DEBUG

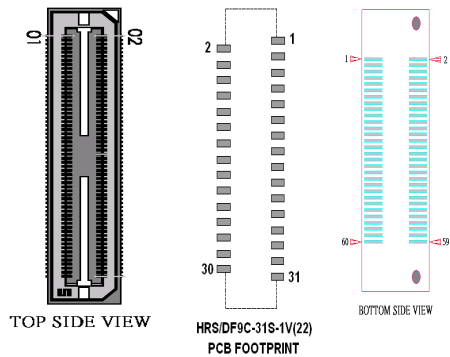
PEGATRON CORPORATION Engineer: XXXX-XX

| Size | Project Name | Rev |
|------|--------------|-----|
|------|--------------|-----|

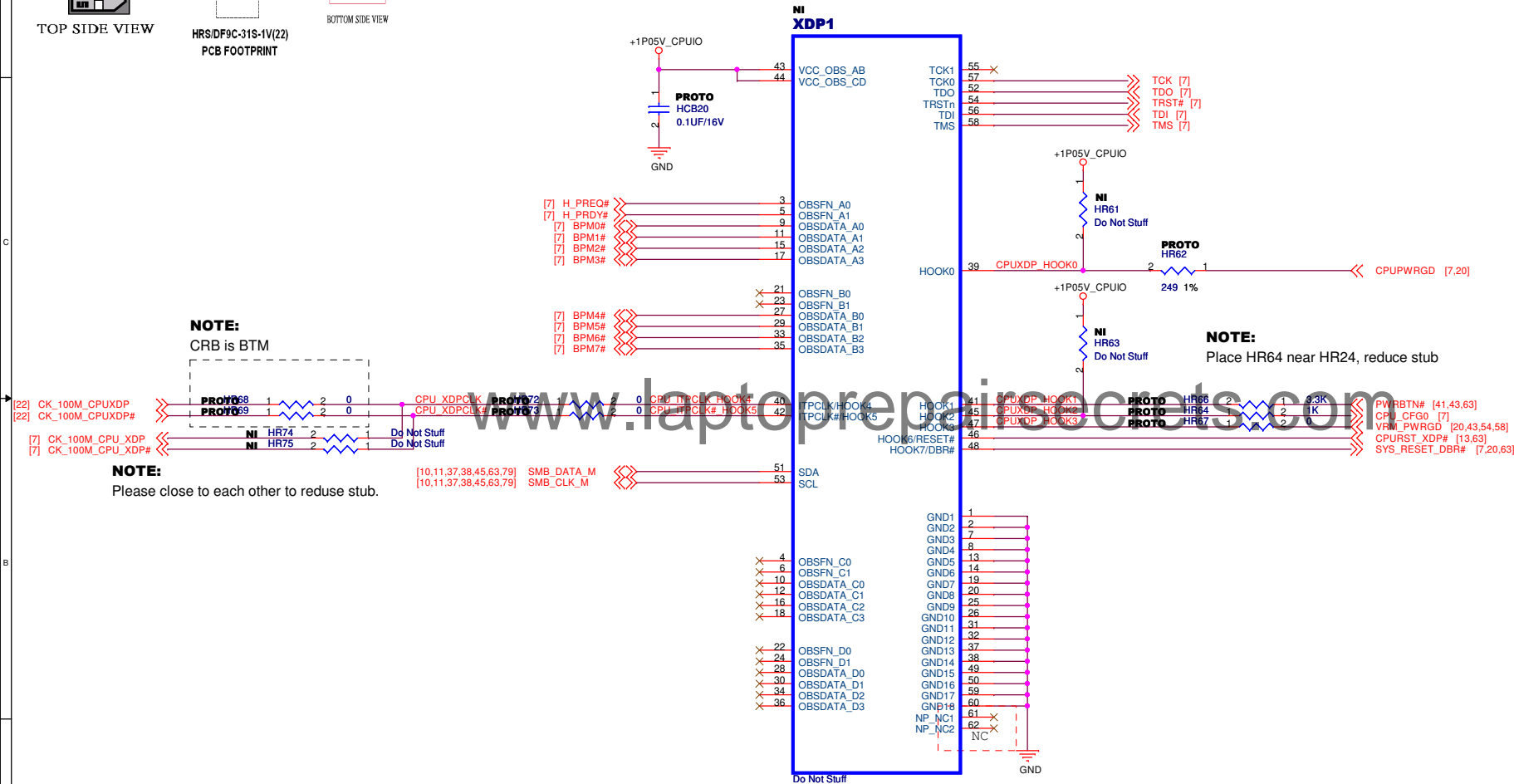
| | | |
|----|----------|-----|
| A3 | IPPSB-FA | 1.0 |
|----|----------|-----|

Date: Wednesday, April 27, 2011 Sheet 63 of 79

| | |
|--|---|
| | 1 |
|--|---|



INTEL CPU XDP DEBUG PORT



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU XDP DEBUG

PEGATRON CORPORATION Engineer: XXXX-XX

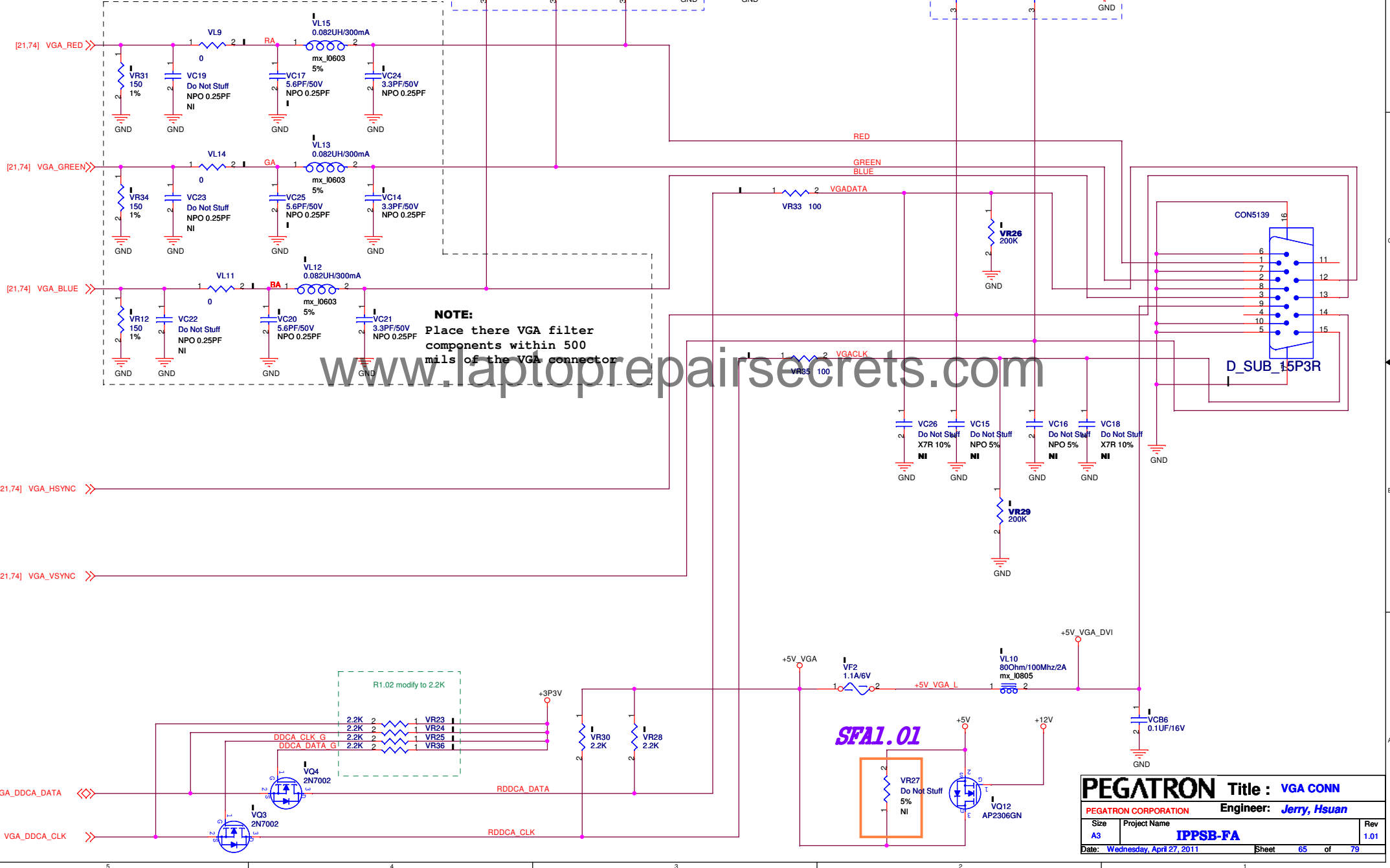
| Size | Project Name | Rev |
|------|--------------|------|
| A3 | IPPSB-FA | 1.01 |

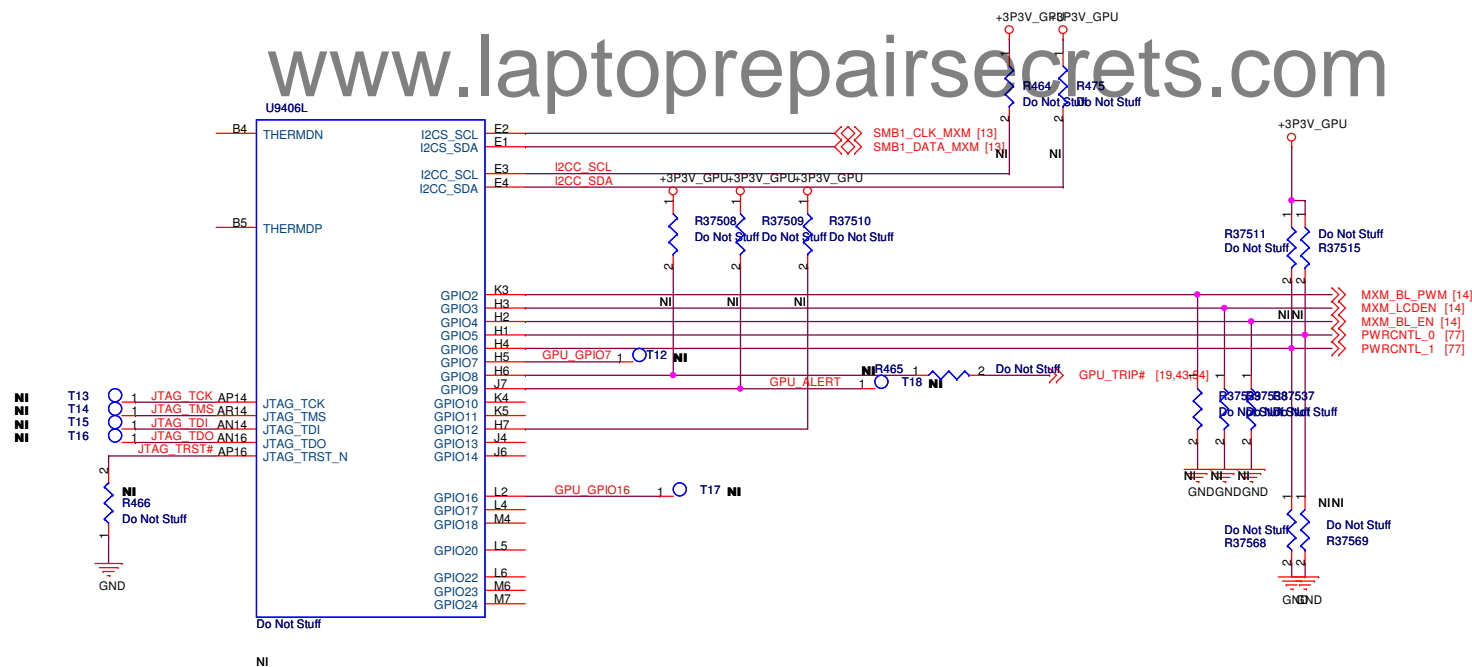
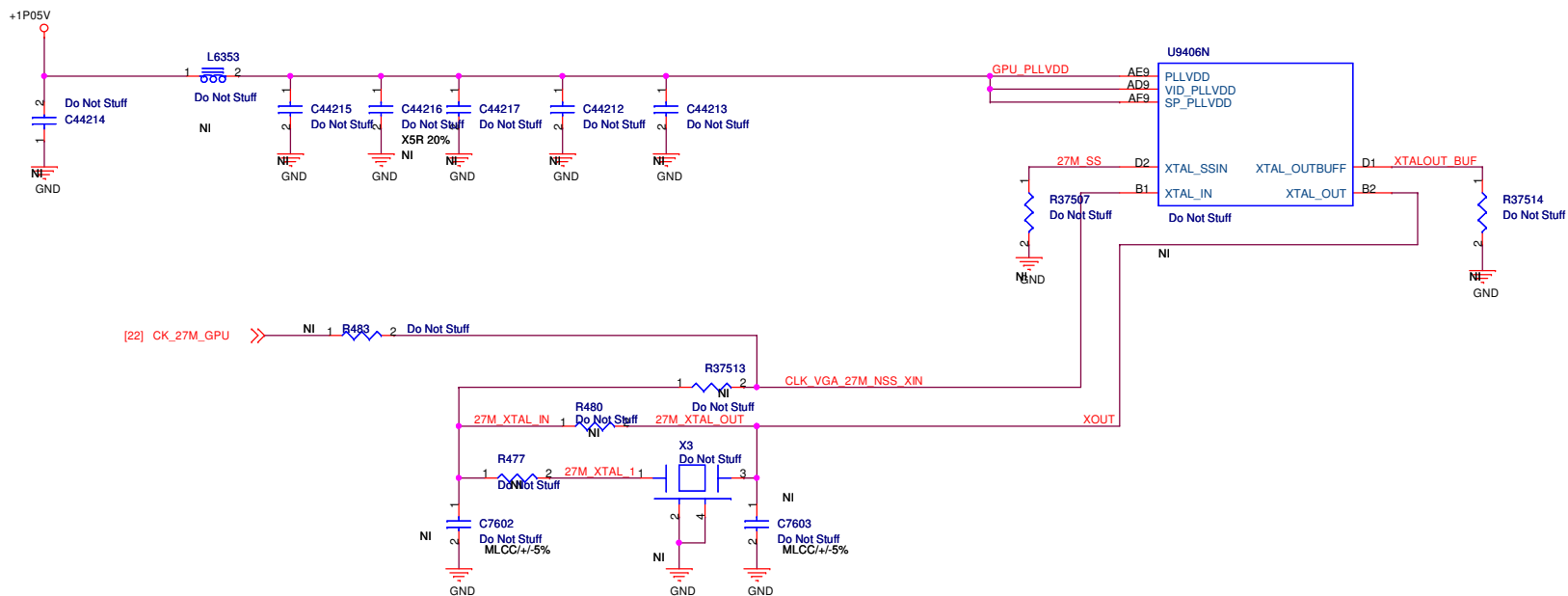
Date: Wednesday, April 27, 2011 Sheet 64 of 79

整份新增修改

Install the VD1/VD2/VD3/VD4/VD5 diode to prevent from ESD issue

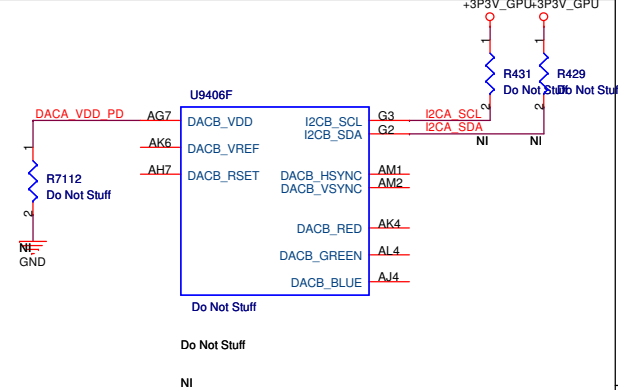
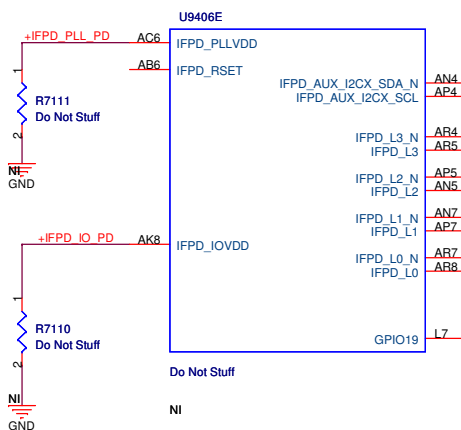
NOTE:



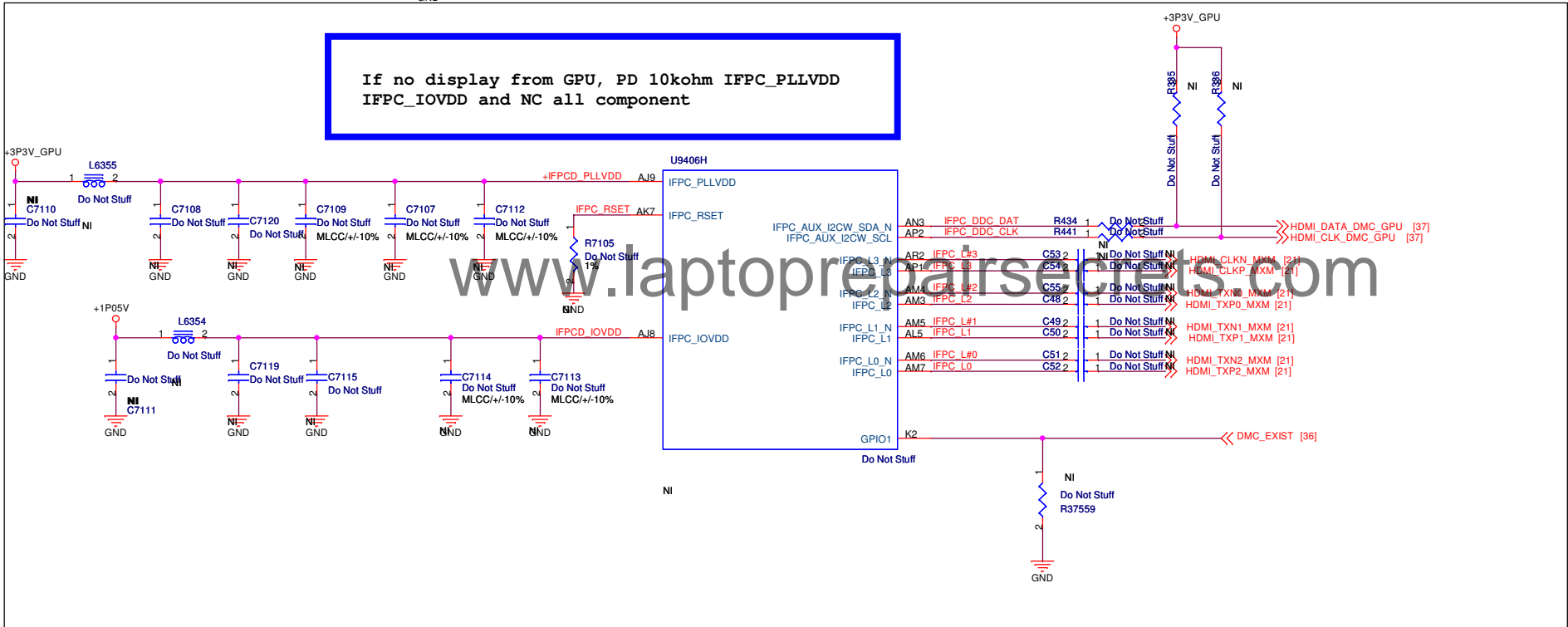


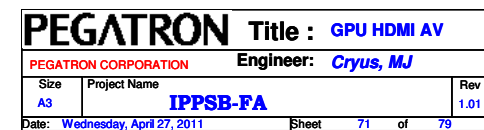
0413

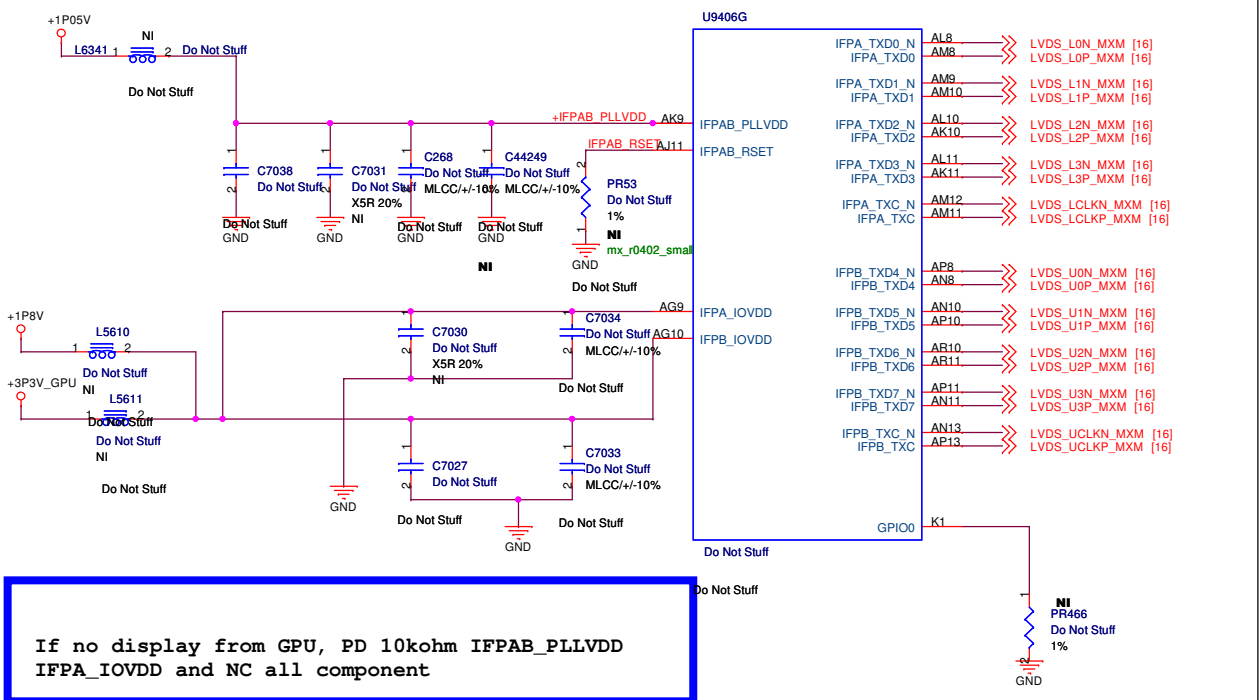
| | | | |
|---------------------------------|--------------------------|--------------------------|-------------|
| PEGATRON | | Title : GPU Xtal/Thermal | |
| PEGATRON CORPORATION | | Engineer: Cryus, MJ | |
| Size A3 | Project Name IPPSB-FA | | Rev 1.01 |
| Date: Wednesday, April 27, 2011 | | Sheet 69 of 79 | |



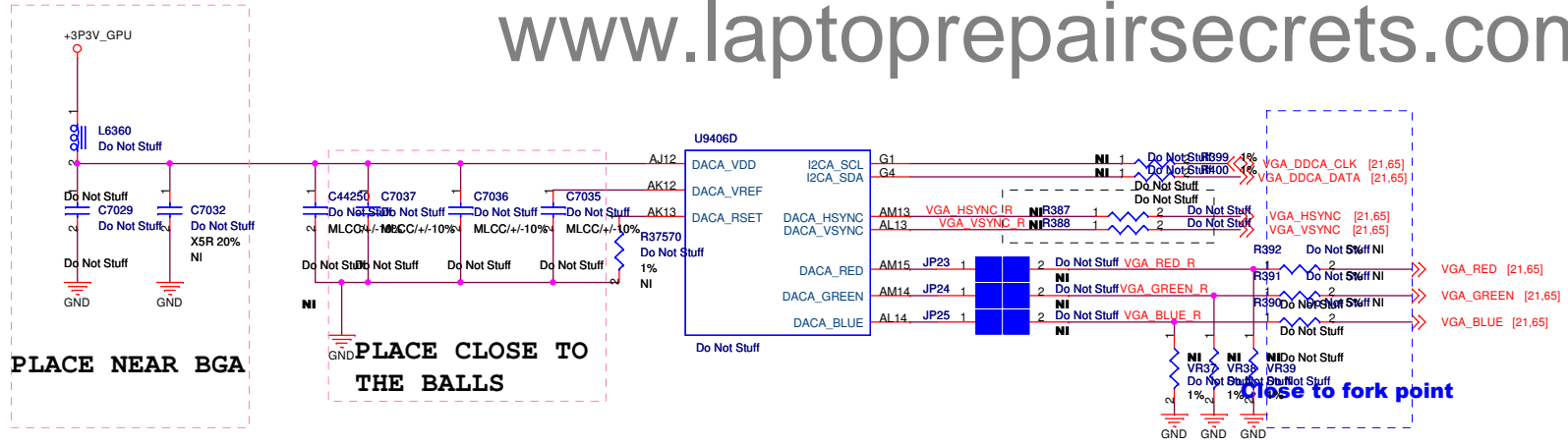
If no display from GPU, PD 10kohm IFPC_PLLVDD
IFPC_IOVDD and NC all component







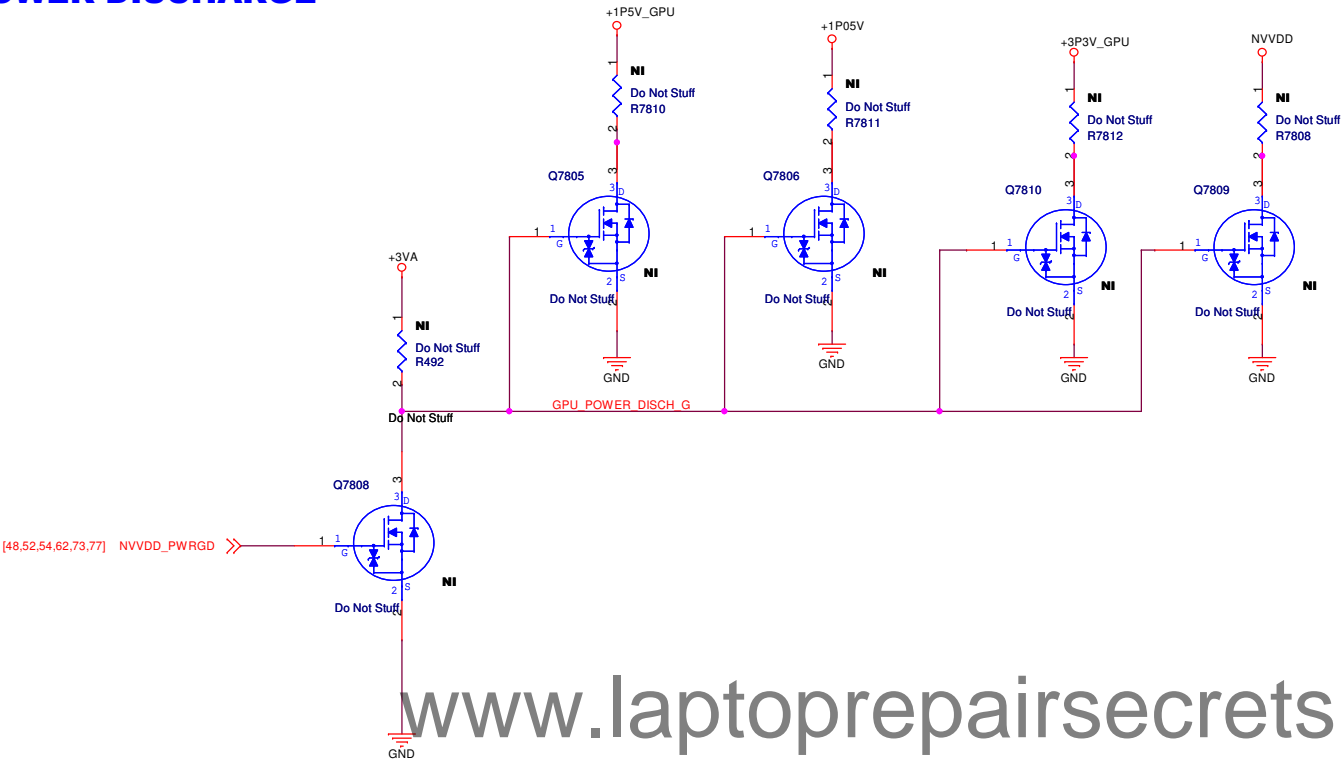
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If no display from GPU, PD 10kohm DACA_VDD ,PU 2.2kohm to +3P3V I2CA_SCL I2CA_SDA and NC all component

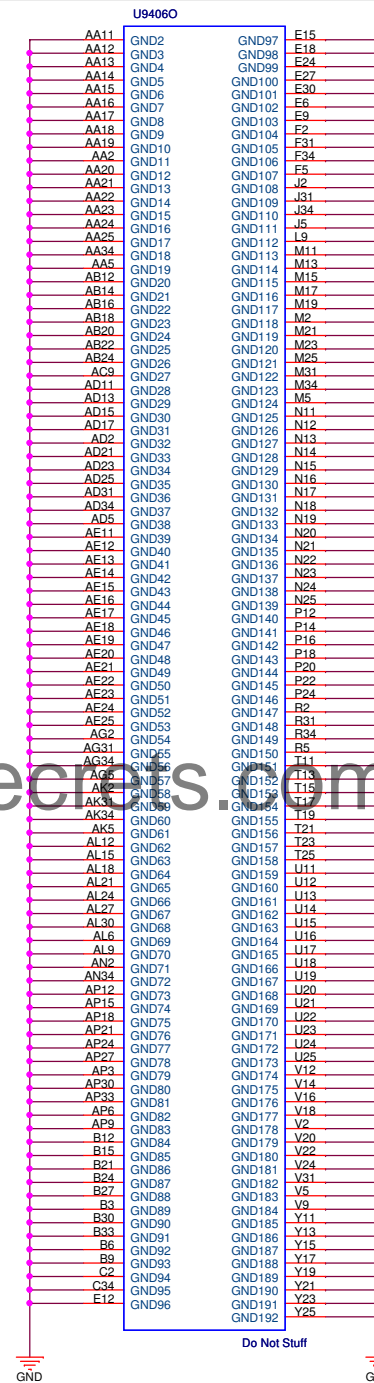
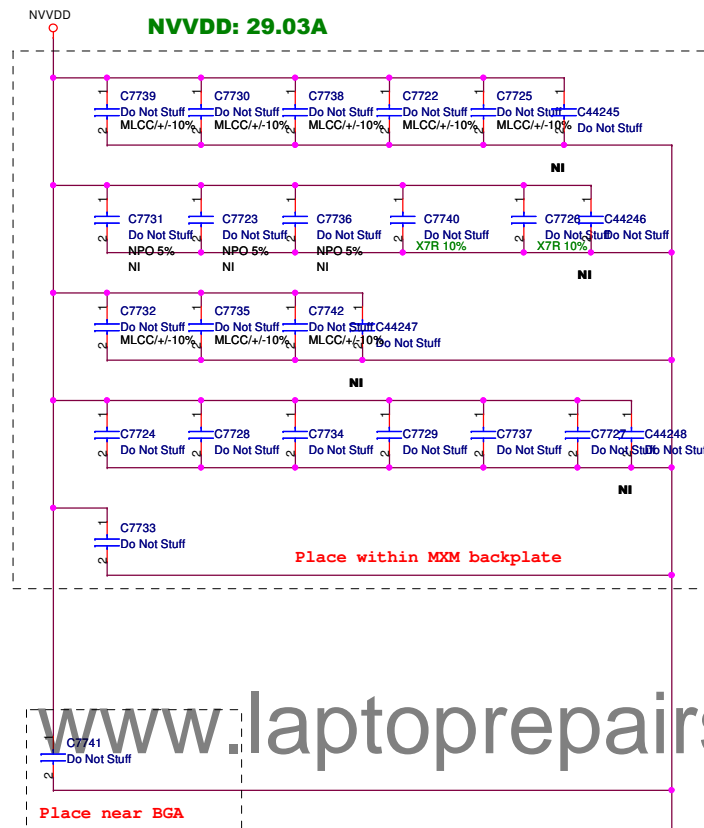
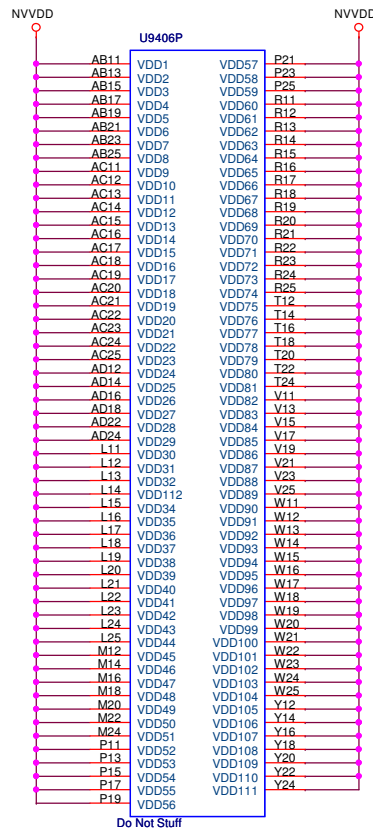
PLACE CLOSE To BALLS

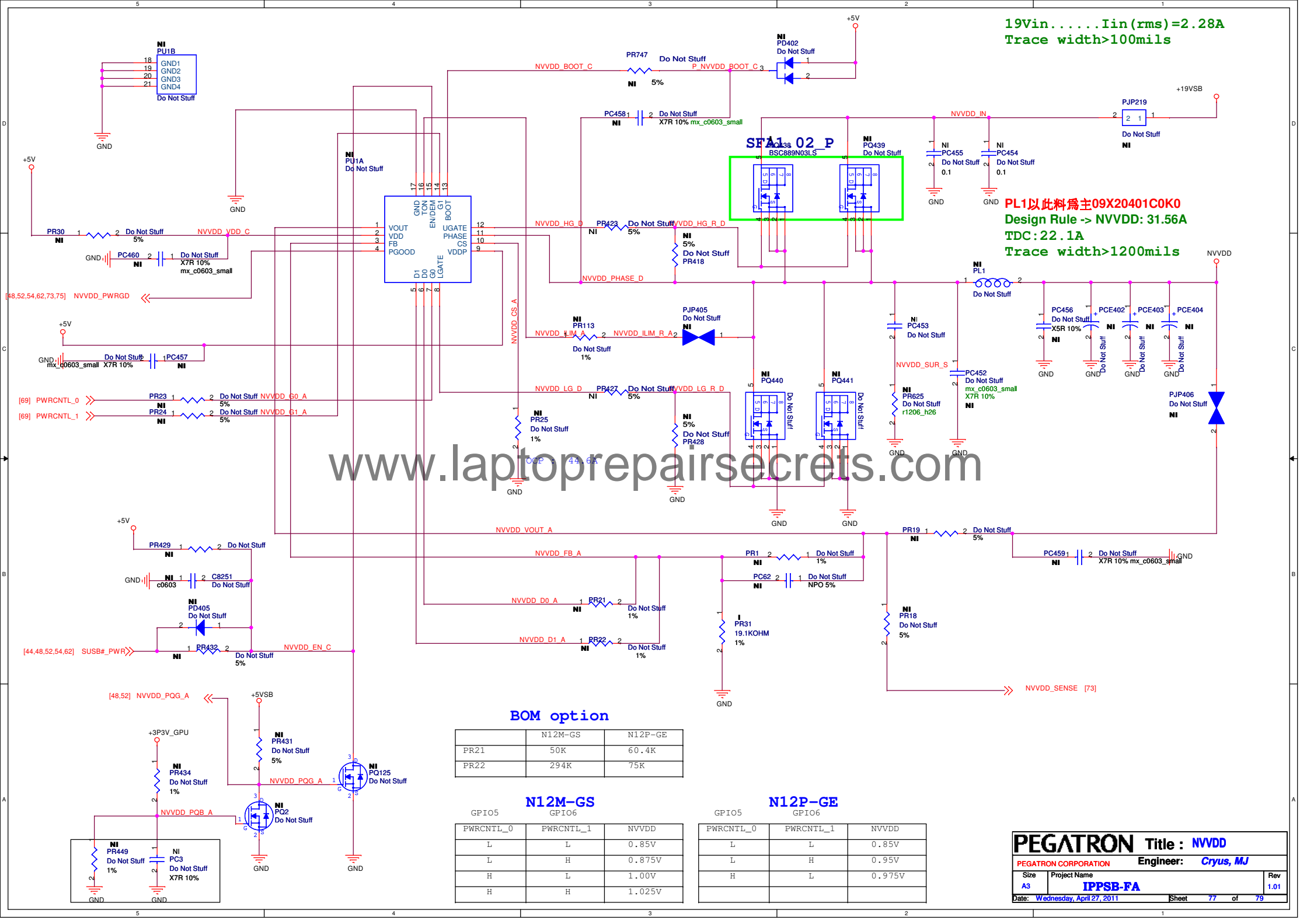
GPU POWER DISCHARGE

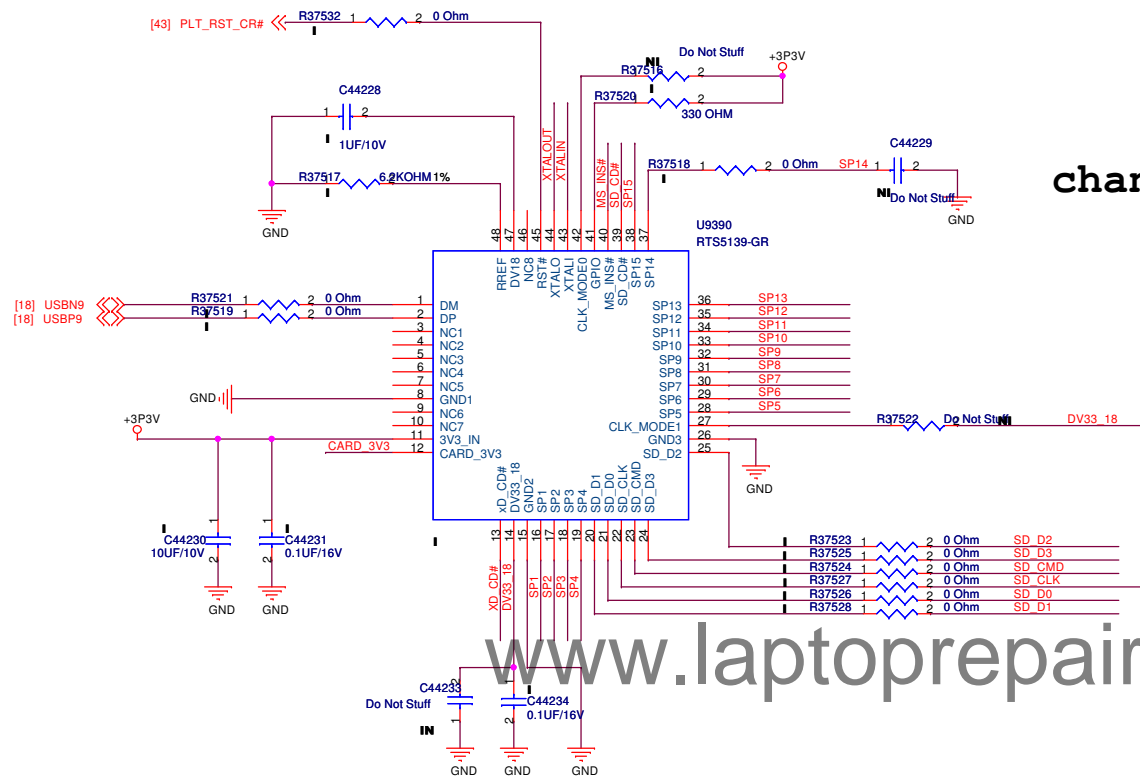


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12/28 新增
01/07 修改

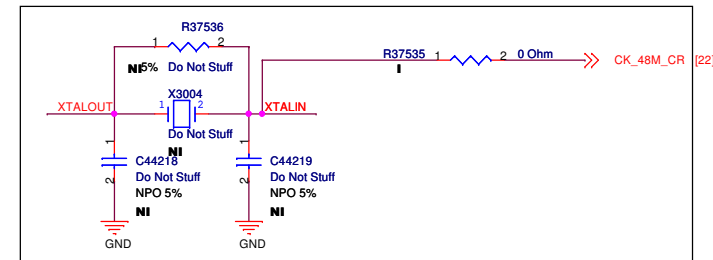






change 48M crystal

SHARE PINGS



| | | |
|------|-------|--------|
| SP1 | SD D7 | XD RDY |
| SP2 | SD D6 | XD RE# |
| SP3 | SD D5 | XD CE# |
| SP4 | SD D4 | XD WE# |
| SP5 | | MS BS |
| SP6 | | MS D5 |
| SP7 | | MS D1 |
| SP8 | | MS D4 |
| SP9 | | MS D0 |
| SP10 | | MS D2 |
| SP11 | | MS D6 |
| SP12 | | MS D3 |
| SP13 | | MS D7 |
| SP14 | | MS CLK |
| SP15 | SD_WP | XD D7 |

Scott CardReader IO

